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FPGA (Field Programmable Gate Array) Technology for Space Communications

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Abstract

Highly reliable aircraft equipment, spacecraft equipment, weapons and military equipment, NPP control systems, medical systems require FPGAs. However, in this direction today develop almost only once-programmable radiation-resistant FPGAs company Actel, which have a triple-bath triggers with a majoritarian scheme of failure suppression and are used in special-purpose equipment.

Keywords: FPGA; control systems; technical; spacecraft.

1. Introduction

The technical and operational characteristics of prospective control and monitoring systems are largely due to the technical level of their FPGAs - electronic nodes, the basis of which implements most interface controllers involved in the transmission and processing of information on board the spacecraft between the processor modules [1]. In addition, an increase in the logical capacity of the FPGA at the present time allows dozens of processor cores or microcontrollers to be implemented on a single chip. At the same time, it is possible to optimize the processor or microcontroller according to the executed commands, which allows to reduce power consumption and increase the clock frequency in comparison with typical microcontrollers [2].

In this connection, the problem of forecasting the radiation resistance of FPGAs operating in the conditions of external radiation factors of outer space is of current importance.

2. Main tasks of the onboard control complex

Due to the harsh conditions of the space environment, increased requirements are imposed on the onboard systems of the spacecraft. Since the vacuum is dangerous for many elements of the spacecraft apparatus, it is necessary to ensure the sealing of the instruments. Also, difficulties arise with the cooling equipment, due to the lack of convection. Sharp temperature drops during the transition from light to shade. All the above listed aspects impose conflicting requirements on the design of the spacecraft.

The design of the spacecraft should be both durable and light, both compact and roomy. The on-board equipment must ensure, with the smallest mass and overall dimensions, the maximum power supply and trouble-free operation [2].

The spacecraft control complex is a combination of instruments and devices with information and software designed to control the movement of the spacecraft and control the operation of the onboard equipment [3].

The main tasks of the BUD are:

- spacecraft motion control;
- spacecraft navigation;
- command and control of service systems and target equipment;
- collection, processing and analysis of control and diagnostic information;
- automatic management of the transition to backup equipment, backup management modes;
- interaction with the ground control complex and crew.

Motion control and navigation task group:

- damping of angular velocity after separation of the spacecraft;
- building the initial solar orientation;
- building and maintaining the orientation of the associated spacecraft axes relative to the reference coordinate systems;
- orbit correction;
- withdrawal of the spacecraft from orbit upon completion of the work;
- definition and forecast of navigation parameters;
- monitoring the performance of instruments and executive bodies used in traffic management and navigation;
- motion control by a motion and navigation control system;
- drive control of solar panels;
- targeting targeted equipment.

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Group of tasks of onboard equipment state control:

- Coordinated management of BS services during ground preparation, autonomous spacecraft functioning and in cooperation with the low-level switchgear assembly and crew;
- command management of service systems and structural elements;
- organization of monitoring and diagnostics of onboard equipment for the purposes of autonomous control, as well as in the interests of the GCC and the crew;
- synchronization of management and control processes by service systems;
- power distribution to onboard consumers;
- calculation of power consumption balance and load shedding management.

The task group of control elements of the structure:

- control of spacecraft after homing;
- management of the disclosure of structural elements (panels SAT and antennas);
- motion control and current orientation of the SC panels to the Sun;
- protection of electrically-explosive devices from untimely operation and from the effects of static electricity.

2.1. Technical review of the existing FPGA controllers

Restoration of FPGA logic after failures in complex and special operating conditions is not currently envisaged, although the technological prerequisites for this have already been created.

1. Identification, description and systematized prevailing types of functional failures of FPGA under the influence of radiation factors of outer space.
2. Offering methods of independent functional control of basic FPGA units, which allows to determine the moment of FPGA functional failure and failed unit, as well as minimizing time and labor costs in the preparation and conduct of radiation tests by creating universal library of FPGA test firmware and corresponding external test units.
3. Offering methods of computational and experimental methods for estimating the cross section of functional failures of devices implemented in FPGAs. The method will allow reducing the volume of experimental studies in the evaluation of the functional failure section of the device implemented in the FPGA and optimizing the functional implementation of the device.

To solve the problem, an analysis of various FPGA models was performed.

1) The MAX II family PLUS is non-volatile (the configuration is stored in the configuration flash memory block) and is ready for operation immediately after power is turned on. Chips of this kind support in-circuit programming mode via JTAG-interfaces. The MAX II kind includes two built-in linear voltage regulators:

MAX II G - core supply voltage 1.8 V;

MAX II Z - core voltage of 1.8 V, ultra-low static power consumption, extended range of housing types [4].

Table 1. Characteristics of PLD family MAX II.

		EPM240/G/Z	EPM2210/G
Resources	Number of logical elements	240	2210
	Number of equivalent macrocells (1)	192	1700
	User Flash Memory (kbps)	8	
	Maximum signal propagation delay from input to output (ns)	4.7 (MAX II/G) 7.5 (MAX II Z)	7
I/O subsystem	Supported I / O Voltage Levels (V)	1.5, 1.8, 2.5, 3.3	
	Number of I / O banks	2	
	Number of output resolution circuits (OE)	80	
	LVTTL / LVCMOS I/O Standards Support	there is	
	32-bit, 66-MHz PCI I/O standard support	there is	
	Schmitt Triggers in I / O Elements	there is	
	Programmable slew rate	there is	
I/O subsystem	Programmable built-in pull-up resistors	there is	1.5, 1.8, 2.5, 3.3, 5.0 (2)
	Conclusions with the "programmable earth" mode	there is	4
	Open drain mode	there is	272
	Bus state hold mode	there is	

2) Altera Cyclone III EP3C10E144C8 FPGA chip from Altera company. It provides the developer with the following resources:

a) Logic elements - 10320;
b) Memory - 414 Kb;
c) Built-in multipliers - 23 (18x18) or 46 (9x9)
d) The number of PLL – 2 [5].

3) FPGAs from the Microsemi SoC company (Actel) are successfully used in GLONASS satellite systems, on the Soyuz, Progress spacecraft and in other complexes requiring increased reliability. For space testing, the Microsemi SoC Antifuse FPGA controller is more reliable; it has the following advantages:

- Low consumption among the chips of this type;
- the absence of the configuration loading stage in the FPGA, the readiness of the FPGA for work on the achievement of the supply voltages of nominal values;
- saving of PCB area due to the lack of CPLD-loader and power monitor;
- the highest reliability confirmed in hundreds of projects - the absence of single failures in the altitude range from 0 to 18,000 m above sea level;
- immunity to configuration failures when exposed to high-energy proton and neutron beams;
- the impossibility of unauthorized reading and modification of the configuration of the FPGA;
- high degree of integration;
- no current surge at power on [6].

Table 2. Characteristics of the FPGA family of Altera Cyclone III.

		Cyclone III (1.2 V core power supply)	
		EP3C5	EP3C120
Resources	Number of logical elements, thousands	5	119
	Num of blocks of the built-in RAM M9K	46	432
	Integrated in RAM (kbps)	414	3 888
	Number of multipliers 18 x 18	23	288
Architectural features	Number of global synchronization circuits	10	20
	PLL blocks	2	4
	Configuration file size (Mbps)	2.8	27.2
	Project copy protection	No	
I/O subsystem	Supported I/O Voltage Levels (V)	1.2, 1.5, 1.8, 2.5, 3.3	
	Supported I/O Standards	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5-V HSTL (I and II), 1.8-V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS	
	Number of LVDS channels emulated	66	229
	Built-in termination resistors (OCT)	Sequential and differential	
	Supported external memory interfaces	QDR II, DDR2, DDR, SDR	

2.2. The principle of operation of orientation devices on the Sun

Devices targeting the Sun are designed for use as part of orientation systems and autonomous navigation of spacecraft. The sensor generates digital signals [7] proportional to the deviation of the direction to the center of the Sun relative to the instrumental coordinate system and, paired with the orientation device to the Earth, allows for three-axis stabilization of the spacecraft in roll, pitch and yaw.

Solar sensors have been used and are being used on almost all spacecraft, starting with the first satellites. The design and principles of their actions are well developed. Further improvement of these devices is made in order to increase reliability and service life, reduce the cost and weight of sensors.

Devices oriented to the Sun have a similar principle of operation to devices oriented to the Earth.

The solar position sensor SDP-1 is an optoelectronic device consisting of two slit optical cameras. Each camera consists of an optical device with a slit mask and a photosensitive element. The dimensions of the slit and the distance between the slit mask and the sensitive plane of the photodetector are selected so that the angular field of view has dimensions 950x50.

The flux of solar radiation entering the input of the optical device is attenuated by light filters and, after passing through a slit mask, falls on the photodetector. The analog electric signal formed in the photodetector under the influence of solar radiation is converted, amplified and supplied to the switching and converting device of the control system, signaling the presence of the Sun in the field of view 950X50.

Two optical cameras, installed at an angle of 900 between the normals to the photosensitive planes of the receivers with overlapping 50 fields of view along the length of the slits, together form a full field of view of 1850x50 and a common area of view of 50x50. The bisector of the angle between the normals to the photosensitive planes of the receivers determines the line of sight of the solar sensor OZп. the line OXp perpendicular to the plane of the normals of the photodetectors and the sighting axis OZp, and the direction OYp, complementing the axis OXp, OZp to the right orthogonal instrument trihedron OXpYnZp, form a flat coordinate system OXpUp. Information about the angular coordinates of the center of the Sun is determined by the state of the output signals of the photodetectors and the fixing of the time of their switching. The direction to the center of the Sun is determined in two stages:

- Rotation of the spacecraft around the axis OXp until the appearance of at least one signal from the photodetector;
- Rotation of the spacecraft around the axis of the CCT until the signal appears from two photodetectors. Fixing in time the moment of switching signals and knowledge of the angular velocity of the rotation of the spacecraft can calculate and memorize the angular coordinates of the center of the Sun in the true or sensory inertial coordinate system. The error in determining the coordinates of the center of the Sun depends on the accuracy with which the switchings are fixed and the angular velocities are taken into account. Conducting special calibration work with the solar position sensor SDP-1 allows to obtain the accuracy characteristics in several angular minutes. The optical camera of each channel of the device orientation to the sun PSD-1 consists of:

  - Neutral filter;
  - slit mask;
  - Photodetector.

- A neutral filter is necessary to attenuate the solar radiation flux entering the input of an optical camera in order to ensure an acceptable level of the photodetector. The neutral filter is performed by vacuum deposition of a metal film on the upper part of K-208 quartz glass and an In_2O_3 layer, which has electrical contact with the instrument case for removing the electric charge. An opaque metal film is applied to the bottom of the quartz glass, on which a slit mask is formed by photolithography. The slit mass is designed to form the illumination when the Sun enters the field of view of the camera. A photodiode is used as a photodetector in an optical camera. The solar position sensor SDP-1 has the following optical parameters:

- Filter transmittance - 1/2500… 1/3000;
- Focal length (distance from the photo-receiving surface to the slit mask) - F = 10.5 mm;
- The width of the gap - 200 microns. The amplification path of the device contains two identical channels that amplify the signal from each

photodiode. Both channels of the photodetector and amplifier are duplicated with cold backup. The signal from the photodiode through decoupling resistance enters the threshold device. When the input voltage exceeds a given level, a high level signal appears at the output. Power is supplied by a constant voltage of ± 12.6 V. A disadvantage of solar position sensors is the impossibility of functioning in the shadow of the Earth.

3. Results and discussion

The validity of the study is confirmed by checking the results of solving the proposed equation of conservation of functional completeness using the developed program, as well as by checking the compliance of the obtained solutions with the Post theorem; verification of the representation of Boolean functions in given bases by calculating the corresponding conjunctions (solving the inverse problem); verification of automatically synthesized circuits using circuit simulation in the system "Quartus II" company Altera; using the proven mathematical apparatus of Boolean algebra, automata theory and the theory of reliability.

Scientific and technical task of developing new and improving the existing methodological and technical means of testing FPGAs for resistance to the effects of radiation factors of outer space in order to predict their radiation behavior in actual operating conditions, allowing to ensure the accuracy of determining the efficiency of FPGAs under conditions of radiation exposure and identify failed functional block.

4. Conclusions

Development of digital circuits using FPGA is the main method of designing complex digital devices. The degree of integration and the frequency range of the FPGA crystals makes it possible to form complex designs of radio equipment blocks based on modern methods of digital signal processing. For mass production of devices, the FPGA project can be transformed into a version of manufacturing chips based on semi-custom arrays or basic matrix crystals, which will reduce the cost. If you want to make changes to the project during operation, the programmable elements of the FPGA allow you to change the internal structure of the chip directly in the system without dismantling the case. The use of formal languages for the description of high-level hardware allows us to increase the efficiency of the development process for space devices.

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