

## Burn-in Test Detection Method for Electronic Products based on VFSA-ELM

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Received 26 May 2018; Accepted 12 September 2018

### Abstract

A burn-in test aims to screen out hidden defects in a circuit generated by the production process. The detection efficiency is mainly affected by factors such as the welding process, circuit board design and detection algorithm. To improve the efficiency of the burn-in test for detection and improve the recognition rate of circuit fault, this study proposed an analogue circuit fault-detection method and burn-in test model in combination with the advantages of simulated annealing and extreme learning machine algorithms. The convergence and search global optimal solution of simulated annealing, and the relationship between the convergence speed, number of hidden layers and extension algorithms of the extreme learning machine was investigated. The results show that the proposed new algorithm can be used for the comprehensive burn-in test of products. The accuracy of fault recognition based on the very fast simulated annealing extreme learning machine algorithm in the failure test of Sallen-Key filter is 92.5%, and the accuracy of incremental extreme learning machine, convex incremental extreme learning machines, and enhanced incremental extreme learning machine algorithms have increased by 2%, 3.3%, and 4.7%, respectively. Meanwhile, Very Fast Simulated Annealing-extreme learning machine has a fast convergence rate and a compact network structure that can reduce the detection time and improve the efficiency of detection. This method can solve the inability of the circuit device to completely function in the burn-in test system and can improve the ability of the product to accurately detect the fault position. This study provides a new reference plan for the burn-in test of electronic products in production lines.

*Keywords:* Product inspection system, Simulated annealing, Extreme learning machine, Soft fault detection in analog circuits

### 1. Introduction

A burn-in test is conducted as a basic assessment of electrical performance in reliability assurance technology. This test identifies the defective products by real-time recording and comparison of the working conditions of the products. Parameters of the functional modules are applied by exposing the products to a specific environment and working condition according to the procedures specified by the testing system [1].

As electronic equipment plays an important role in production, medical care, and military operations, the application requirements of related technologies such as burn-in tests are gradually increasing due to the growing demand for reliable equipment in various fields. Related technological research has advanced as numerous research institutions and companies participate in all aspects of research, design, production, and application. Most burn-in tests are geared toward integrated circuits. For example, American company Teradyne, the world's largest automatic test equipment manufacturer, developed a comprehensive component ultra-large-scale integrated test system called Integra J750 [2]. Furthermore, China Beijing Huafeng Test & Control Technology Co. Ltd. established the STS 2103B semiconductor discrete device test system. However, the system for detection of analog circuits and electronic

products has not been involved in their burn-in test research [3]. To perform automatic online detection, Shenzhen University developed an electronic product burn-in method based on RS485 bus using microcontroller MSP430 as the core. However, due to the limited processing capacity of the microcontroller, the method cannot handle a large-scale burn-in test; it can only test the product function but cannot detect analogue circuit faults [4].

Nevertheless, with the continuous development of devices for the Internet of Things, smart devices based on embedded systems have been applied in key areas such as medical services and urban lighting construction. Therefore, detecting circuit components in the burn-in test of such products has become a comprehensive task. To detect as many components as possible on the circuit board, a neural network algorithm based, for example, extreme learning machine (ELM), incremental extreme learning machines (I-ELM), is added to the burn-in test system to establish a fault model of the analog circuit. The associated fault model involves many factors and technical difficulty but also brings great potential for the research on burn-in tests [5].

Based on these findings, we conducted in-depth research on the fault detection of analogue circuits. Using the aforementioned literature [6-9], we found that the simulated fault detection algorithm based on the extreme learning machine is superior in accuracy, training time, and detection time. Other classic analogue-circuit diagnostic methods, except the related algorithms, are still characterized by low accuracy and long test time. In addition, the structure of the training model is not compact in the simulation circuit-

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doi:10.25103/jestr.114.05

detection experiment. Thus, increasing the convergence rate of the extreme learning machine algorithm and avoiding the local trap are urgent problems to be solved.

To achieve these objectives, the present study obtains the root mean square (RMS) value of the node voltage as the training sample by circuit simulation of each fault in the analogue circuit at each frequency, as well as the convergence and number of hidden layers and the implicit neuron bias parameters of the algorithm of the extreme learning machine. The relationship between the input layer parameters is analyzed, as well as the characteristics of the simulated annealing algorithm in searching for the global optimal solution. The aim is to improve the convergence speed of the extreme learning machine algorithm to avoid falling into local optima, and to apply this algorithm to the burn-in test system to perform fault detection of the analog circuit. This step completes the automatic test of the burn-in test for electronic products.

## 2. State of the art

Research on the reliability of electronic products began in the early 1950s through a series of studies conducted by the US military and industry to solve the reliability problems of military electronic equipment [10]. At present, a key technical problem in the burn-in test of electronic products is how to conduct performance testing on all components of the finished product. In the actual production process, the main integrated circuit chips are individually tested, but the analog boards that work with them are difficult to put through separate burn-in tests. Thus, the fault detection of the analog circuit is a key issue.

In recent years, researchers have done considerable work on fault detection of analogue circuits. Burdick [11-12] used time domain sensitivity analysis to study the tested circuit; then, he used the difference between the normal working state and output response of each fault state as the optimization function to select the test excitation frequency, but the number of linear test vectors increased with the number of faults and the implementation was poor. Variyam et al. [13-14] generated test excitations for linear analogue circuits through fast fault simulation algorithms based on state-space representation and adjugate matrix, but these were not relevant for nonlinear electric circuits. Han et al. [15-16] used the improved classification speed as the optimization target, and classified the potentially faulty components by using the modified Mahalanobis distance according to the characteristic values of the measuring points. However, the detected and diagnosed faults are characterized as soft faults with large variations in analogue circuit parameters. These parameters are mainly concentrated on soft faults where the component parameters deviate from the normal tolerance range by 50% or more. For example, Zhu et al. [17-19] applied Fourier transform and wavelet transform to a probabilistic neural network consisting of four layers (including input and output), but their approach also introduced the Monte Carlo method with very large computational complexity. Luo et al. [20-21] proposed a fault diagnosis method based on the network tearing method and combined it with analog neural network fault diagnosis; however, this method can only solve the large-scale analog circuit by direct current voltage output diagnosis. Long et al. [22-24] proposed a feature vector selection method based on Mahalanobis distance, but this

method suffers from slow network convergence and easily converges to the local optimal value.

The preceding research results are mainly from the theoretical study of analogue circuit faults, and few studies have focused on circuit fault detection in electronic product burn-in tests. Therefore, in view of the limitations of existing research, the present study uses the circuit simulation of each fault in the analogue circuit to obtain the RMS value of the node voltage as a training sample at different frequencies. Then, this study analyzes the relationship between the convergence and the number of hidden layers in the related derivative algorithm for the extreme learning machine. An in-depth study of the perturbation method of the simulated annealing algorithm is required to find the optimal solution. By combining the fast convergence speed of the extreme learning machine algorithm and the very fast simulated annealing algorithm, we can search for the characteristics of the global optimal solution. The VFSA-ELM algorithm is proposed to solve the slowness of network convergence and the easy convergence to the local optimal value. The model is introduced into the burn-in test system to further detect the failure of the analog circuit as well as complete the automatic control and product screening of the burn-in test of the electronic product.

The rest of this study is organized as follows. Section 3 presents the algorithm model of the very fast simulated-annealing extreme learning machine and the software flow of the burn-in test system. Both models are based on the large-data-volume message conversion technology. Section 4 compares the performance of the very fast simulated annealing extreme learning machine algorithm with other extreme learning machine algorithms through different database tests. This approach combines the test data to analyze the advantages and disadvantages of each algorithm. Section 5 then summarizes the conclusions.

## 3. Methodology

Figure 1 presents a functional diagram of the electronic product for the burn-in test system. The system consists of an operation interface, a strategy control, a judgment module, a message conversion system, and a TCP/UDP server.

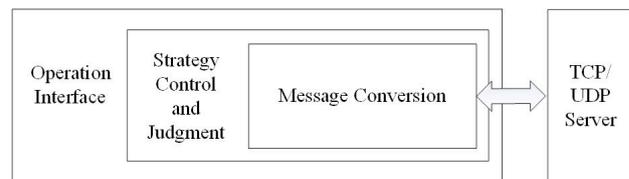


Fig. 1. System function diagram

The operation interface is an important part of user interaction, as a good user interaction environment improves user efficiency. The operation interface mainly allows selection and detection of the storage strategies, addition and deletion of tested product IDs, and execution of test instruction, preservation and other functions of the test results. Thus, the interface is easy to read and operate. Strategy control and judgment provide the system with the ability to read and store strategies and automatically judge the detected data. The soft fault detection of the circuit board is realized by training the RMS voltage data at different frequencies, which are detected by the extreme learning machine. The message conversion system is the core structure of this detection system. This system implements functions including packet conversion and packet

reconfiguration and then completes the mapping relationship of multi-platform message conversion. According to the test process, the system always issues the working instructions of the relevant functions during the burn-in test. The relevant functional operations are always conducted in the electronic equipment. The relevant working parameters are then reported to the system and the function of the product burn-in test is realized by comparing the data features.

### 3.1 Extreme learning machine

An extreme learning machine is a new type of feedforward neural network called single hidden-layer feedforward network (SLFN). Its algorithm can overcome the limitations of multiple iterations in classical neural network algorithms during training. Only a simple linear regression is required to obtain relatively satisfactory requirements. This approach produces good outcomes and faster training time [25].

Huang et al. [26] conducted an in-depth study on the finite set input of feedforward neural networks and found that for the finite set of  $Q$  different samples, if the activation function of the feedforward neural network is an infinitely differentiable function of arbitrary intervals, then the hidden layer of SLFNs requires up to  $Q$  neurons to be able to approach the  $Q$  samples infinitely. This finding also shows that the learning ability of SLFNs is independent of the weight of the input layer to the hidden layer. This condition only relates to the weight of the hidden layer to the output layer. To address this issue, Huang et al. designed a new type of feedforward neural network called extreme learning machine.

The network structure diagram of SLFNs is shown in Figure 2. ELM is composed of an input layer, a hidden layer, and an output layer similar to SLFNs. The input layer, and only one hidden layer and output layer, are fully connected through neurons.

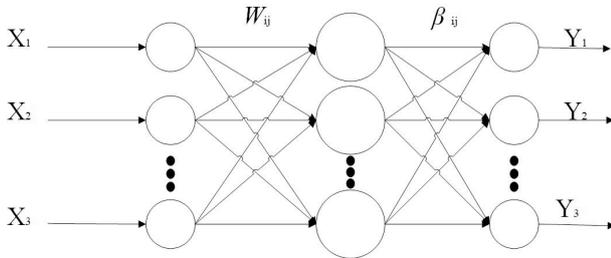


Fig. 2. Network diagram of ELM

When the input layer has  $n$  neurons and the hidden layer has 1 neuron, the connection weight  $w$  of the input layer and the hidden layer is expressed as follows:

$$W = \begin{bmatrix} w_{11} & w_{12} & L & w_{1n} \\ w_{21} & w_{22} & L & w_{2n} \\ L & L & L & L \\ w_{l1} & w_{l2} & L & w_{ln} \end{bmatrix}_{l \times n} \quad (1)$$

where  $w_{ji}$  represents the connection weight of the  $i_{th}$  neuron of the input layer and the  $j_{th}$  neuron of the hidden layer.

When the output layer has  $m$  neurons, the hidden layer has 1 neuron, and the connection weight  $\beta$  of the output layer neurons and the hidden layer neurons is as follows:

$$\beta = \begin{bmatrix} \beta_{11} & \beta_{12} & L & \beta_{1m} \\ \beta_{21} & \beta_{22} & L & \beta_{2m} \\ L & L & L & L \\ \beta_{l1} & \beta_{l2} & L & \beta_{lm} \end{bmatrix}_{l \times m} \quad (2)$$

where  $\beta_{jk}$  represents the connection weight of the  $j_{th}$  neuron of the hidden layer and the  $k_{th}$  neuron of the output layer.

When the threshold  $b = [b_1 \ b_2 \ L \ b_l]^T$  of the hidden layer neurons is set, the training set input matrix and the  $Y$  output matrices with  $Q$  samples are established.

Then, according to Figure 2, the output  $T$  of the network is  $T = [t_1 \ t_2 \ L \ t_Q]_{m \times Q}$ , so each vector  $t_j$  in the  $T$  matrix is

$$j = \begin{bmatrix} t_{1j} \\ t_{2j} \\ M \\ t_{mj} \end{bmatrix} = \begin{bmatrix} \sum_{i=1}^l \beta_{i1} g(w_i x_j + b_i) \\ \sum_{i=1}^l \beta_{i2} g(w_i x_j + b_i) \\ M \\ \sum_{i=1}^l \beta_{im} g(w_i x_j + b_i) \end{bmatrix} \quad (j=1,2,\dots, Q) \quad (3)$$

Where  $w_i = [w_{i1} \ w_{i2} \ L \ w_{in}]$ ,  $X_j = [x_{1j} \ x_{2j} \ L \ x_{nj}]^T$ ,  $g(x)$  is an excitation function that can be "Sigmoid," "Sine," and so on.

The above formula (3) can be written as  $H\beta = T'$ , where  $T'$  is the transposition of the matrix  $T$ , and  $H$  is the output matrix of the ELM hidden layer. Therefore, the specific form of  $H$  is as follows:

$$H = \begin{bmatrix} g(w_1 x_1 + b_1) & g(w_2 x_1 + b_2) & L & g(w_l x_1 + b_l) \\ g(w_1 x_2 + b_1) & g(w_2 x_2 + b_2) & L & g(w_l x_2 + b_l) \\ L & L & L & L \\ g(w_1 x_Q + b_1) & g(w_2 x_Q + b_2) & L & g(w_l x_Q + b_l) \end{bmatrix}_{Q \times l} \quad (4)$$

In fact, the number of neurons in the hidden layer is unlikely to be equal to the number of training samples. Let  $E$  be the sum of the squares of the errors of the ELM. Therefore, the optimal value of the network weight finally solved is such that  $E = \|H\beta - Y\|$ . The value is the smallest.

Huang et al. [27] provided the following two theorems by studying SLFNs, which is the theoretical basis for the realization of ELM.

Theorem 1: Given any  $Q$  different samples  $((x_i, t_i))$ , where  $x_i = [x_{i1} \ x_{i2} \ L \ x_{in}]$ ,  $x \in R$ ,  $t_i = [t_{i1} \ t_{i2} \ L \ t_{in}]$ ,  $t \in R$ , and when the activation function  $g(x)$  is infinitely differentiable in arbitrary intervals, arbitrarily assigning  $w_i \in R$  and  $b_i \in R$ , then for SLFNs with  $Q$  hidden layer neurons, the hidden layer matrix  $H$  is reversible, and  $\|H\beta - T'\| = 0$ .

Theorem 2: Given any  $Q$  different samples  $((x_i, t_i))$ , where  $x_i = [x_{i1} \ x_{i2} \ \dots \ x_{in}]$ ,  $x \in R$ ,  $t_i = [t_{i1} \ t_{i2} \ \dots \ t_{in}]$ ,  $t \in R$ , given arbitrary small error  $\varepsilon > 0$ . When the activation function  $g(x)$  is infinitely differentiable in any interval, arbitrarily assigning  $w_i \in R$  and  $b_i \in R$ , then for SLFNs with  $K$  ( $K < Q$ ) hidden layer neurons, the hidden layer matrix  $H$  is reversible, and  $\|H\beta - T'\| < \varepsilon$ . Through the above theorem, extreme learning determines the weight of the output layer by training the sample [28].

The solution of the equation by the method of least squares is

$$\hat{\beta} = \arg \min \|H\beta - Y\| = H^+ Y' \quad (5)$$

where  $H^+$  is the Moore–Penrose generalized inverse matrix of the hidden layer matrix  $H$  as follows:

$$H^+ = (H^T H)^{-1} H^T \quad (6)$$

The algorithm of the extreme learning machine is divided into the following three steps:

- (1) Determining the number of neurons in the hidden layer, randomly setting the connection weight  $w$  of the input layer, hidden layer, and threshold  $b$  of the implicit neuron;
- (2) Selecting an infinitely differentiable function as the activation function of the hidden layer neurons, and then calculating the hidden layer output matrix  $H$ ;
- (3) Calculating the output layer weight  $\hat{\beta}$ .

### 3.2 Very Fast Simulated Annealing (VFSA)

Simulated annealing (SA) algorithm is a combined optimization algorithm that iterates the Metropolis algorithm. The name is based on the fact that the algorithm simulates the solid annealing process.

In the SA algorithm, the control parameter of the optimization problem is assumed to be a temporary solution, and the non-negative objective function is equivalent to a microscopic state of a solid at a certain temperature and its energy. The control parameter, whose value is decremented by the algorithm process, is also assumed to be equivalent to the temperature of the solid annealing process state. For each value of the control parameter, the algorithm continues to perform the iterative process of “generating a new solution–judging–accepting or discarding,” which corresponds to the process of solids approaching thermal equilibrium at a constant temperature, i.e., implementation of a Metropolis algorithm [29].

The SA algorithm uses the Metropolis algorithm to generate a sequence of solutions of combined optimization problems. The transition probability corresponding to the Metropolis criterion assumes that the current state  $\chi_{old}$  is transformed from the  $\chi_{old}$  to  $\chi_{new}$  by some perturbation. At the same time, the energy of the system is also changed from  $E(\chi_{old})$  to  $E(\chi_{new})$ , and therefore, the probability of system transformation is

$$p = \begin{cases} 1 & \text{if } E(\chi_{new}) < E(\chi_{old}) \\ \exp\left(-\frac{E(\chi_{new}) - E(\chi_{old})}{T}\right) & \text{if } E(\chi_{new}) \geq E(\chi_{old}) \end{cases} \quad (7)$$

The basic idea of SA is as follows:

(1) Initialization: random generation of a starting solution  $\omega$ , so that the starting temperature is  $T(0) = T_0$  (sufficiently large); the starting state of the initial solution is  $S$ ; and the algorithm processes any  $T$  value under the repetition number  $L$  (Markov chain length) to calculate the value of the objective function  $f(\omega)$ ;

(2) Generating a new solution  $\omega_{best}$  based on the existing optimal solution  $\omega'$  on a neighborhood function and then calculating the new objective function value  $f(\omega')$ ;

(3) Deriving the value of the change of the objective function  $\Delta f = f(\omega') - f(\omega)$  from the evaluation function  $f(\omega)$ ;

(4)  $\Delta f < 0$  is accepted as the latest optimal solution  $\omega'$  and, in addition, the probability of acceptance calculated by the Metropolis algorithm is chosen as the newest optimal solution  $\omega'$ ;

(5) If  $c = \text{random}[0,1] < p$ ,  $\omega_{best} = \omega'$ ; or  $\omega_{best} = \omega_{best}$ ;

(6) If the current temperature is greater than the minimum set temperature, and the number of iterations is less than the Markov chain length, then execute step 2;

(7) Once the current parameters have met the pre-set stop conditions, the algorithm stops and outputs the current solution  $\omega'$  as the optimal solution; the stop conditions generally stop the algorithm if the new solution is not accepted after multiple consecutive attempts;

(8) The temperature decreases and the process returns to step 2.

The specific steps are shown in Figure 3. The cooling schedule refers to a process management table that gradually drops from a higher temperature  $T_0$  to a lower temperature. Based on the assumption that the temperature at time  $t$  is represented by  $T(t)$ , the cooling formula used by the traditional SA algorithm is as follows:

$$T(t) = \frac{T_0}{\lg(1+t)} \quad (8)$$

VFSA approach is similar to the conventional VFSA approach. The difference is that the very fast annealing method uses a temperature-based Cauchy rule step-by-step method [30] in the perturbation solution. The formula is as follows:

$$a_{k+1}^i = a_k^i y^i (B_i - A_i) \quad (9)$$

$$y^i = \text{sgn}(u - 1/2) T_i [(1 + 1/T_i)^{2|u-1|} - 1] \quad (10)$$

In Eq. (9),  $K$  is the current number of iterations;  $a_k^i$  is the  $i_{th}$  parameter of the current number of iterations;  $u$  is  $[0,1]$ , a random number according to the cloud distribution;  $A_i$  and  $B_i$  are the upper and lower bounds;  $a_{k+1}^i$  and is the value after the disturbance.

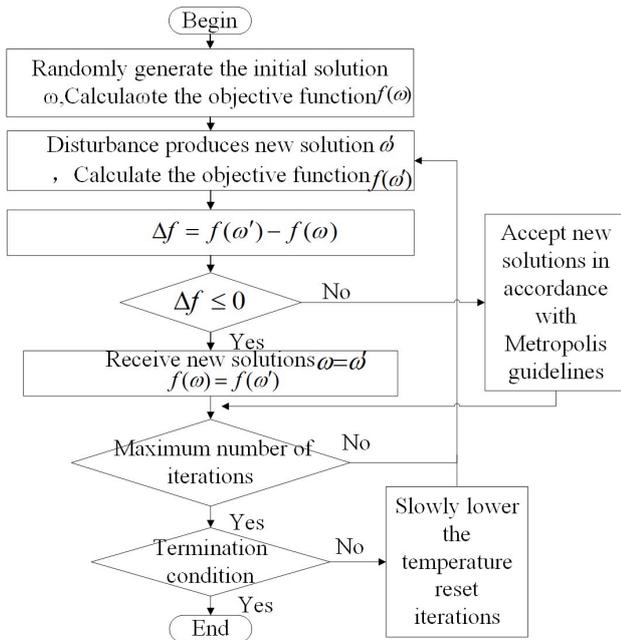


Fig.3. Flowchart of simulated annealing algorithm

### 3.3 VFSA-ELM

Since the traditional extreme learning machines determine that the number of hidden layers is artificially based on experience. This study proposes to use a VFSA approach to optimize the ELM algorithm, and to explore the optimal hidden layer number and the optimal model by using simulated annealing. The initial temperature is set to the maximum number of hidden layer nodes, and the perturbation solution is a matrix composed of input weight vector and hidden layer offset value. The error value of E can be E for actual output and expected output. The specific steps are as follows:

(1) Initialization: initial number of hidden layers, initial solution  $\omega$ , repetition number  $L$  (i.e., Markov chain length) under any  $T$ -value in the algorithm, and calculation of the objective function value  $E$ ;

(2) Generating new solutions according to formula (9) and calculating  $E'$  and  $\Delta E = E(\omega') - E(\omega)$ ;

(3) When  $\Delta E < 0$  is accepted as the newest optimal solution  $\omega'$ , the probability of acceptance calculated by the Metropolis algorithm becomes the newest optimal solution;

(4) If  $c = \text{random}[0,1] < p$ ,  $\omega_{best} = \omega'$ ; or  $\omega_{best} = \omega_{best}$ ;

(5) If the current temperature is greater than the minimum set temperature, and the number of iterations is less than the Markov chain length, execute step 2;

(6) Once the current parameters have met the pre-set stop conditions, the algorithm stops and outputs the current solution  $\omega'$  as the optimal solution; the stop conditions generally stop the algorithm if the new solution is not accepted after multiple consecutive attempts;

(7) According to formula (8), the temperature decreases, and the process returns to step 2.

### 3.4 Particle turbulence operation

The system flowchart is shown in Figure 4. When the device under test is connected to the message conversion system module through the TCP or UDP protocol, the module registers and starts waiting for the operator of the interface management system to issue commands. Following the

relevant detection of instructions, the interface management system module divides the issued instruction into three groups: parameter setting array, product sequence number array, and policy array. Then, the module establishes a test table in the interface according to the product serial number array and the policy array, in which these arrays are sent to the strategy control and judgment module. The arrays are subsequently assembled into a policy message array according to the policy array and sent to the message conversion system module together with the product sequence number array. The message conversion system module converts the transmitted message into a corresponding binary message, allowing the TCP/UDP service module to send the message to the corresponding test device through the server for system detection. Meanwhile, the parameter setting array is sent to the data strategy control and judgment module, waiting for the return message once the test device has been examined. When the message of the tested equipment is generated, it is sent to the TCP/UDP service module. The TCP/UDP service module subsequently converts it to the message conversion system module according to the reported binary message, and then converts the message into a JSON report. Thereafter, the message is placed in the data strategy control and judgment module, and the parameters returned by the device are judged according to the parameter setting array. The circuit detection mechanism in the strategy control and judgment module is based on the VFSA-ELM algorithm for learning and modeling. Therefore, according to the given voltage data, the algorithm can automatically detect circuit soft faults. The judged data are sent to the interface management system module to perform the corresponding display, enabling the staff to judge and save the data [31].

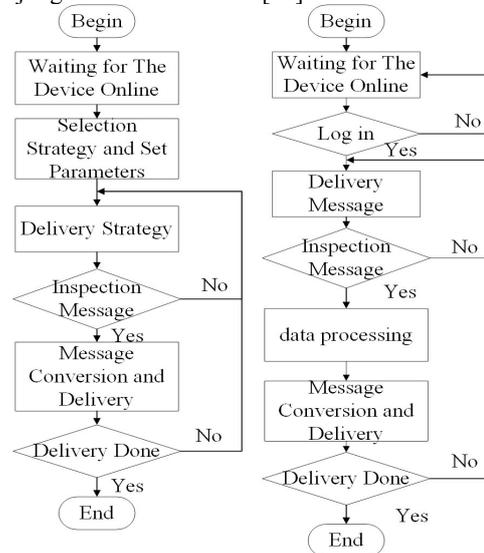


Fig. 4. Flowchart of general function

## 4 Result Analysis and Discussion

### 4.1 Comparisons with VFSA-ELM

In this study, the algorithms VFSA-ELM, I-ELM, convex incremental extreme learning machines (CI-ELM), and enhanced incremental extreme learning machine (EI-ELM) all use the Sigmoid function as excitation function. To conduct a comparative test, we use six groups of standard data: Abalone, Boston Housing, California Housing, Delta Ailerons, Delta Elevators, and Parkinson's. The expected value error predicted for selection information of the specific data is shown in Table 1.

**Table 1.** Predicted data expected value error

Dataset	Abalone	Boston Housing	California Housing	Delta Ailerons	Delta Elevators	Parkinson's
Expected Error $\epsilon$	0.13	0.13	0.19	0.05	0.06	0.09

**Table 2.** Errors in ELM algorithm for six sets of standard data tests

	I-ELM	CI-ELM	EI-ELM	VFSA-ELM
Abalone	0.095	0.094	0.078	0.087
Boston Housing	0.137	0.135	0.136	0.129
California Housing	0.191	0.095	0.190	0.011
Delta Ailerons	0.052	0.048	0.057	0.033
Delta Elevators	0.067	0.032	0.069	0.040
Parkinson's	0.090	0.087	0.089	0.056

**Table 3.** Comparison table of training time of different ELM algorithms for different data (unit: sec)

	I-ELM	CI-ELM	EI-ELM	VFSA-ELM
Abalone	0.059	0.020	0.101	1.498
Boston Housing	0.017	0.011	0.022	2.059
California Housing	0.148	0.144	1.878	4.565
Delta Ailerons	0.040	0.002	0.069	1.898
Delta Elevators	0.050	0.007	0.198	3.221
Parkinson's	0.038	0.010	0.049	5.454

Table 2 demonstrates the comparison of several ELM algorithm errors for the six sets of standard data tests. The table shows that the error of CI-ELM is the smallest in the Delta Elevators dataset. In other cases, the error of VFSA-ELM is slightly less than that of other ELM algorithms. Therefore, in this test, the error rate of VFSA-ELM is generally better than that of other ELM algorithms.

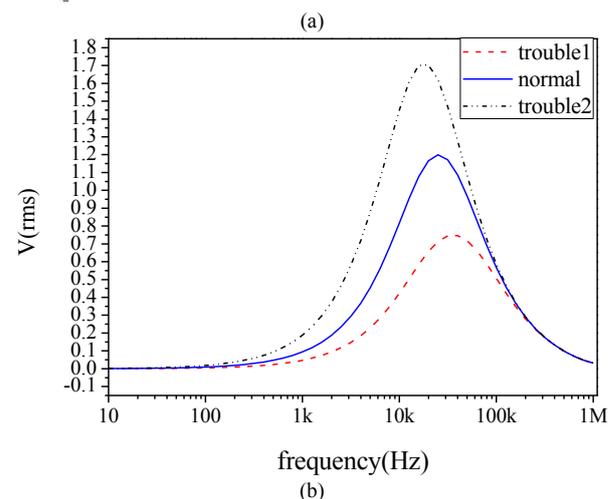
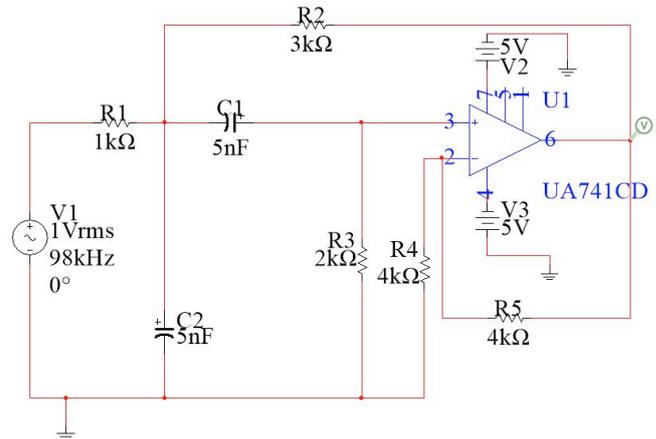
Table 3 presents the training time of different ELM algorithms. According to the table, the CI-ELM training time is relatively short, the VFSA-ELM training time is significantly higher than that of other algorithms, but the training time is still within the acceptable range.

According to the tests of the aforementioned algorithms, the VFSA-ELM has a low error rate. Although the training time is longer than that of other algorithms, it is within the acceptable range for burn-in testing. Therefore, VFSA-ELM with higher accuracy is used as the training model algorithm for the circuit fault detection of the burn-in test.

#### 4.2 Burn-in test

The main circuit of the intelligent street-lighting control terminal in the burn-in detection object is a system board based on STM32 microcontroller design, which is essentially an analog control circuit. Therefore, this study lists part of the system board circuit Sallen-Key filter for its fault analysis. Figure 5(a) shows the Sallen-Key filter; when a problem occurs in one of the layers (C1, C2, R1, R2, and R3), it is assumed to have a strong impact on the overall circuit. Figure 5(b) shows the influence of R3 normal and fault on the output voltage; thus, the corresponding output voltage is obtained as the model parameter of fault diagnosis by exciting various components in the circuit at different frequencies.

Owing to an excessive number of sampling parameters for different frequencies, the learning rate and training accuracy of the next ELM are affected. Therefore, this study uses principal component analysis to reduce the dimensionality of sample features.



**Fig. 5.** Diagram of circuit fault detection. (a) Schematic of Sallen-Key filter. (b) Voltage output curve of resistance R3

The test errors of the different hidden layers in the VFSA-ELM, I-ELM, CI-ELM, and EI-ELM networks are shown in Figure 6. Notably, the convergence speed of VFSA-ELM is faster than that of I-ELM, CI-ELM, and EI-ELM. Thus, we can conclude that the network structure of VFSA-ELM is relatively simple and compact in training and testing.

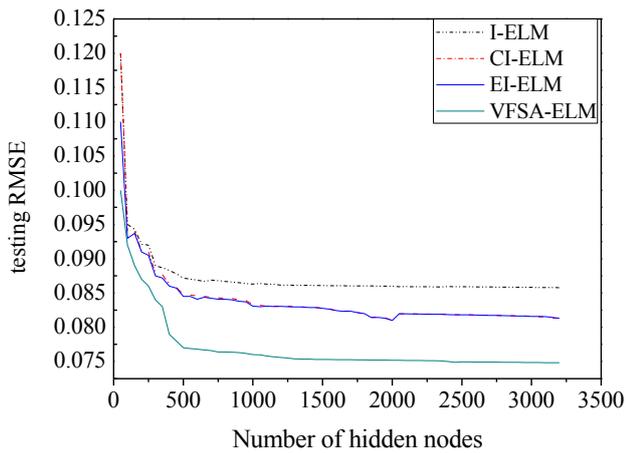


Fig. 6. Comparison of VFSA-ELM, I-ELM, CI-ELM, and EI-ELM network on Sallen-Key failure

Figure 7 displays the system interface. The test results are compared by issuing the function of the burn-in test of the smart street-lighting controller device with known fault conditions. Prior to the start of the test, the controller should

be co-located in the same local area network as the test computer. Figure 8 presents the test stand of the burn-in. When the test terminal is connected to the power supply device and the signal generator, the terminal system automatically connects to the tested LAN through the wireless network card. When the burn-in system detects the terminal device, the burn-in command is automatically issued.

The method has high accuracy and can meet the requirements of the burn-in test. At the same time, the method meets the requirement for the burn-in test to automatically issue test functions to multiple devices and automatically discriminates the product faults. By monitoring the system log and analysis of data loss during the network transmission process by the third-party software, we found that the high error rate was due to packet loss or delay during network transmission, resulting in false positives caused by false positives. By improving the ELM algorithm, the error rate of the circuit fault detection of the burn-in test system is considerably reduced. Although the training time is not better than that of other ELM algorithms, it is better than that of the other ELM algorithms in the burn-in detection system.

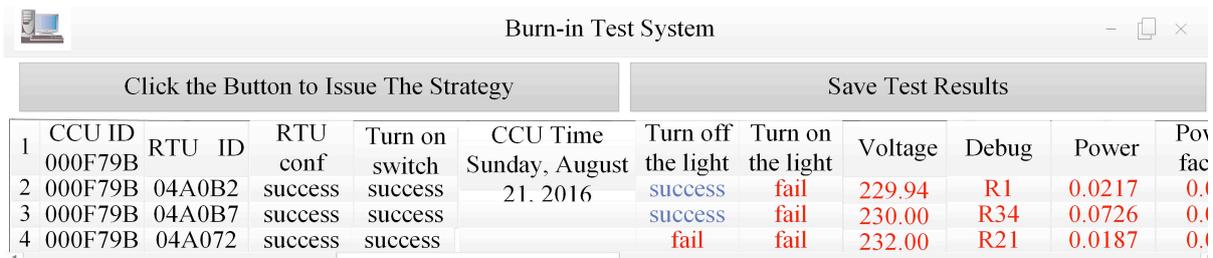


Fig. 7. Interface of testing results display

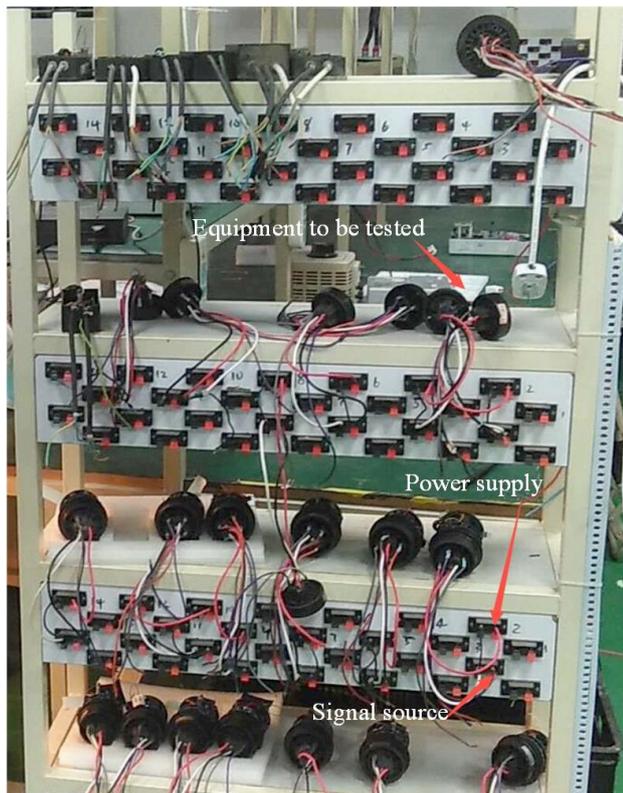


Fig. 8. Test stand of the burn-in

## 5. Conclusions

To solve the problems in the test such as low accuracy of the analogue circuit test, incomprehensive inspection of components, and inability to perform large-scale batch inspection, this study started with the analogue circuit detection method and analyzed the VFSA-ELM algorithm. The following conclusions could be drawn:

- (1) The ELM easily falls into the local optimal solution because the input parameters and hidden-layer offset values are randomly generated. This phenomenon can be avoided by simulating the annealing method quickly to select its value.
- (2) The model perturbation of the VFSA algorithm uses the Cauchy rules, which greatly improve the convergence speed of the traditional SA algorithm and the convergence speed based on SA-ELM.
- (3) Testing the failure of the Sallen-Key filter showed that the fault identification accuracy of the VFSA-ELM was higher than that of the I-ELM, CI-ELM, and EI-ELM algorithms, and the convergence speed was faster than that of the aforementioned three algorithms. The network structure of VFSA-ELM was relatively simple and compact.

In this study, the production line of the burn-in test is combined with theoretical research, and a new fault diagnosis model for circuit faults in the burn-in test is proposed. The fault diagnosis model is based on the VFSA-ELM algorithm, which solves the inability of the traditional burn-in test to fully detect the circuit board components.

This method provides a new reference scheme for the burn-in test of electronic products in the production line. The fault circuits currently tested are faults caused by a single component. The diagnosis of multiple device faults in the circuit needs further investigation.

Universities (JK2015032) and Xiamen University of Technology (YKJCX2016007).

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#### Acknowledgements

This work was supported by the Fujian Provincial Department of Education Funded Projects for Provincial

#### References

1. Fu, G. C., Chen, Y., Zhang, S. J., "Electronic component reliability technology tutorial". Beijing: Beijing University of Aeronautics and Astronautics Press, China, 2010, pp.1-20.
2. Luo, W., Wei, J. Z., Yang, H., "Electronic component reliability test project". Beijing: Electronic Industry Press, China, 2005, pp.23-56.
3. Zhang, Q. S., "Selection and testing of electronic components". Beijing: Mechanical Industry Press, China, 2003, pp.70-123.
4. Zhang, B., "Design and Implementation of an Electronic Product Burn-in Test System". *Industrial Control Computer*, 20(8), 2007, pp.13-14.
5. Chen, W. J., "FPGA-Based Integrated Circuit Burn-in and Electrical Characteristics Test System Design". Master thesis of University of Science and Technology Liaoning, China, 2016, pp.45-64.
6. Liu, M. R., Zeng, L. He, Y. G., "Analog circuit fault diagnosis based on LMD multi-scale entropy and extreme learning machine". *Journal of Electronic Measurement and Instrumentation*, 31(04), 2017, pp.530-536.
7. Chen, S.W., Liu, G.F., Ye, S., "Research for analog circuit fault diagnosis based on ELM optimized by bat algorithm". *Electronic Measurement Technology*, 38(02), 2015, pp.138-141.
8. Gao, K., "Based on multi-nuclear co-space model of extreme learning machine clustering diagnosis methods research". Master thesis of University of Hunan University, China, 2015, pp.22-27.
9. Zhou, J. Y., "Research on Analog Circuit RUP Prediction Method". Master thesis of University of Electronic Science and Technology, China, 2015, pp.20-110.
10. Wang, X.J., "Quality and reliability in the development of weapons". *Electronic Product Reliability and Environmental Testing*, (6), 2006, pp.41-45.
11. Burdick, B., "Generation of optimum test stimuli for nonlinear analog circuits using nonlinear - programming and time-domain sensitivities", In: *Design, Automation & Test in Europe Conference & Exhibition (2001)*, Munich, Germany: IEEE, 2001, pp.603-609.
12. Burdick, B., "The qualitative form of optimum transient test signals for analog circuits derived from control theory methods". In: *IEEE International Symposium on Circuits and Systems*, Phoenix-Scottsdale, AZ, USA:IEEE, 2002, pp. I-157-I-160.
13. Variyam, P. N., Chatterjee, A., "Specification-Driven Test Design for Analog Circuits". In: *International Symposium on Defect and Fault-Tolerance in Vlsi Systems*, Austin, TX, USA: IEEE Computer Society, 1998, pp.335-340.
14. Variyam, P. N., Hou, J., Chatterjee, A., "Test Generation for Analog Circuits Using Partial Numerical Simulation". In: *International Conference on Vlsi Design - vlsi for the Information Appliance*, Goa, India :IEEE, 1999, pp.597-602.
15. Han, H., Wang, H. J., Bing, L., "Method for analog circuit fault diagnosis based on improved Mahalanobis distance". *Control & Decision*, 28(11), 2013, pp.1713-1717+1727.
16. Han, H., Wang, H. J., Yang, C. L., "A New Method for Analog Circuit Fault Diagnosis Based on Slope Characteristics". *Measurement & Control Technology*, 33(1), 2014, pp. 34-37.
17. Zhu, W.j., He, Y.G., "A New Fault Feature Extraction and Diagnosis Method of Analog Circuits". *Journal of Hunan University (Natural Sciences)*, 38(4), 2011, pp.41-46.
18. Zhu, W.j., He, Y.G., "A neural-network-based fault diagnosis approach for analog circuits by using wavelet transformation and fractal dimension as a preprocessor". *World Academy of Science Engineering & Technology*, 23(68), 2010, pp.571-578.
19. Zhu, W.J., "A Neural-Network-Based Fault Diagnosis Method of Analog Circuits and Its Application". Master thesis of University of Hunan University, China, 2012, pp.30-40.
20. Luo, K. L., He, Y.G., "A Interval Diagnosis Approach of Soft-Fault Diagnosis for Large-Scale DC Analog Circuit". *Journal of Computer-Aided Design & Computer Graphics*, 24(2), 2012, pp.271-278.
21. Luo, K. L., "The Research on Soft-fault Diagnosis of Large-scale Analoge Circuits". Master thesis of University of Hunan University, China, 2012, pp.10-40.
22. Long, B., "Feature Vector Selection Method Using Mahalanobis Distance for Diagnostics of Analog Circuits Based on LS-SVM". *Journal of Electronic Testing*, 28(5), 2012, pp.745-755.
23. Yang, C., Tian, S., Long, B., "Application of Heuristic Graph Search to Test-Point Selection for Analog Fault Dictionary Techniques". *IEEE Transactions on Instrumentation & Measurement*, 58(7), 2009, pp.2145-2158
24. Han, H., Wang, H., Tian, S., "A New Analog Circuit Fault Diagnosis Method Based on Improved Mahalanobis Distance". *Journal of Electronic Testing Theory & Applications*, 29(1), 2013, pp.95-102.
25. Zhang, R., Lan, Y., Huang, G.B., "Universal approximation of extreme learning machine with adaptive growth of hidden nodes". *IEEE Transactions on Neural Networks and Learning Systems*, 23(2), 2012 , pp.365-371.
26. Huang, G., Huang, G. B., Song, S., "Trends in extreme learning machines: A review". *Neural Networks the Official Journal of the International Neural Network Society*, 61(C), 2015, pp.32-48.
27. Huang, G.B. Zhu, Q.Y., Siew, C.K., "Extreme learning machine: a new learning scheme of feedforward neural networks". In: *2004 IEEE International Joint Conference on Neural Networks*, Budapest, Hungary: IEEE , 2004, pp.985-990.
28. Huang, G.B., Ding, X., Zhou, H., "Optimization method based extreme learning machine for classification". *Neurocomputing*, 74(1), 2010, pp.155-163.
29. Metropolis, N., Rosenbluth, A. W., Rosenbluth M.N., "Equation of state calculations by fast computing machines". *The journal of chemical physics*, 21(6), 1953, pp.1087-1092.
30. Chen, H.G., Li, L.H., Xu, H.P., "Modified Very Fast Simulated Annealing Algorithm". *Journal of Tongji University(Natural Science)*, 34(8), 2006, pp.1121-1125.
31. Lin, T.L., Jia, P.L., "The Design and Implementation of Navigation Software System Based on Qt Technology". *Control Engineering of China*, 22(5), 2015, pp.992-995.