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A Simple and Noble Technique for Signal Integrity Test

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Abstract

Purpose of this paper is to describe a noble technique for signal integrity test. Signal integrity is one of the most preferred topics in digital circuit design. It involves the quality degradation and timing errors of digital signal waveforms as they travel on conductors like PCB traces, package structures and interconnects. This paper describes noise immunity and signal shape tests for a back plane signal track used for SDH network.

Keywords: Signal Integrity (SI), Back plane, LVDS signal, PCB.

1. Introduction

Now a days thousands of gates in high-speed digital systems are switched on simultaneously. Due to this switching noise is generated, this noise may affect the signal integrity in a system. All digital gates in a PCB are connected to power supply and a reference plane. The resonance mode of the power planes gets activated when this simultaneous switching noise contains dominant mode of frequency that coincides resonance frequency of the power plane.to mitigate the simultaneous switching noise by reducing the power plane resonance [2]. Modern digital system are capable of providing higher bit rates with low voltage swing [3]. A multilayered Printed Circuit Board forms cavity by parallel planes. When signal is wandering through some layer or plane then it will be greatly affected by the noise from cavity [4]. The current through the via in PCB layer and simultaneous switching of digital system are the main cause of this unwanted noise. [5]. There are various technique have been proposed and implemented to suppress this noise. One such biggest achievement to reduce this noise by using Electromagnetic Band-Gap (EBG) structures [6]. In this type of structure, cavity is formed with regular pattern above or below the solid line of PCB. There is particular frequency band in which the signal does not propagate [7]. Apart from EBG structure other signal Integrity techniques are s Copper/cobalt (Cu/Co) metaconductor based coplanar waveguide (CPW) transmission lines at K-bands and millimeter wave frequencies such as low conductor loss, reduced signal dispersion, and low noise figure[8-9].Effects of termination, clock traces ,length of trace on signal integrity have been vividly discussed in paper [10].Improper termination of high speed buses may cause ringing and stair stepping which results false triggering and data errors [11]. For better and successful signal integrity some simulation methods were suggested based on electromagnetic models[12]. The most promising and accurate signal integrity is based on some complex occurrence like current distribution and dispersion effects [13-14]. A simple arrangement of interconnections and connectivity of different devices is shown in figure 1.there is communication between two devices Device 1 and device 2. Here signal is wondering through different layers pf PCB, integrated circuit (IC) and the package. Usually, vias, bends, and solder balls represents the interconnection. There may be losses of signal travelling through long path due to the impedance change in line. While designing a perfect PCB, trace width must remain same from one end to another end for uniform impedance so as to get considerable dispersion and dissipation effects.

There should be minimal distance of the different traces in PCB in order to avoid the crosstalk effect for better signal integrity the cross talk should be avoided with the help of proper design rules.

2. Signal Integrity Test Set up

The device under test (DUT) is taken a backplane of one SDH product with different daughter card to be plugged into the back plane. Depending upon requirement during signal integrity test, the back plane is loaded or unloaded condition that means daughter cards are plugged or unplugged condition. The test set up is shown in figure 2. The start-up and measurement procedure is as follows: The modules in the back-plane positions are placed as shown Figure 2. Then an optical STM-4 transceiver in the first SFP position is placed in position 1 and 2. The SDH test-set for optical STM-4 measurements is initialized and it is connected to transceiver. Then the pulse generator is connected to the point under test via the home-made probe. The pulse amplitude is increased until errors occur on the test set. This set up basically shows how to measure noise immunity of an internal 100 ohms differential LVDS transport signal. Rise and fall times are defined to be 2ns, which is the fastest that can be provided by the used Pulse generator. Pulse period is defined to be 490ns, the duty-cycle is typical around 10% and the amplitudes are in the range 0.5V to 8V depending on the tests. If nothing else is mentioned then the 3.9nF + 261ohm probe has been used and the amplitude is simply increased until an BER of 10E-9 is reached. The Oscilloscope shown in the test setup serves

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the purpose of checking the probe ratio, which should be around 1:10. The concept has been taken from some white paper[15].

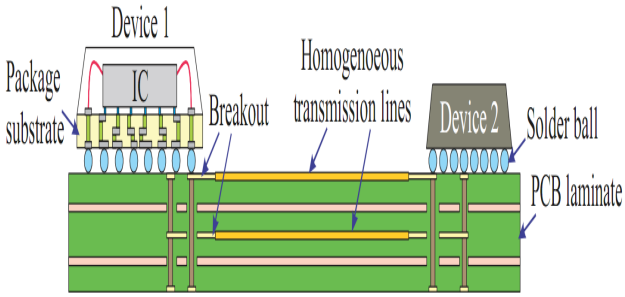

Fig.1. Schematic diagram of PCB with some tracks

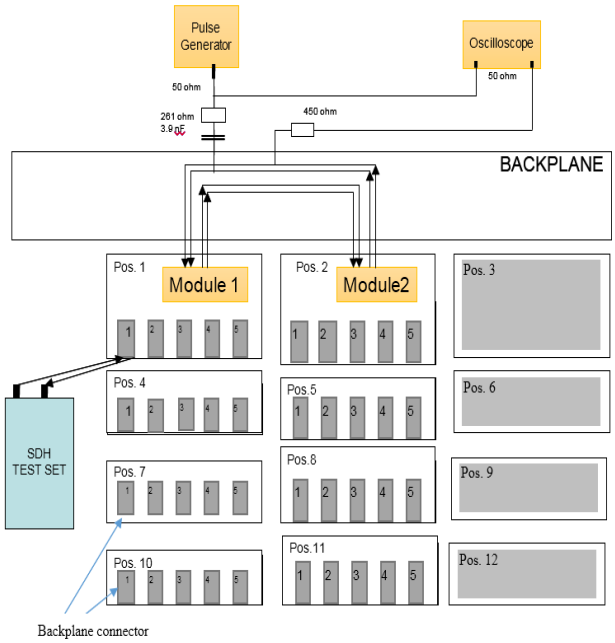

Fig. 2. Test Set up for Signal Integrity

3. Signal Integrity Test results

Fig 3 below shows the generated pulse influence on a 100 ohm LVDS line with the 3.9nF + 261ohm probe. A pulse of around 2V at the generator output gives approximately 200mV on the LVDS line (probe factor 1:10).

Fig. 4 shows generated pulse Influence on standard CMOS with the 3.9nF + 261ohm probe. A pulse of around 2V at the generator output gives approximately 250mV.

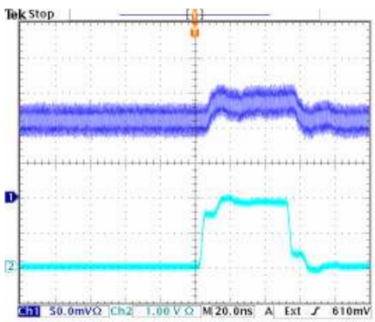

Fig. 3. Generated pulse and influence on LVDS lines, Channel 2 represents generated pulse, channel 1 represents influence on LVDS line

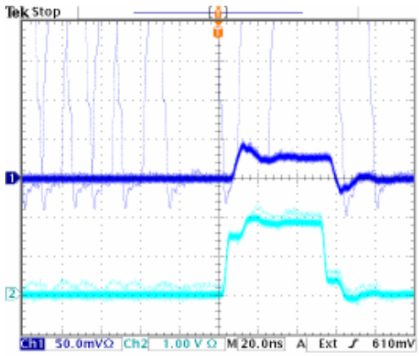

Fig.4. Generated pulse and influence on CMOS lines, Channel 2 represents generated pulse, channel 1 represents influence on CMOS line

Here the noise immunity margin is taken at least 0.7Vor 700mv pulse amplitude with a 3.9nF + 261ohms probe. The noise immunity for both the cases are in acceptable range, which implies better signal integrity in the Device Under Test (DUT).

To verify that the Address lines are not influenced by other signals or have a large reflection from the way as they are routed in the backplane, the chip select line (CS) is active. Oscilloscope probe is connected to chip select (CS) line and to an address line. Setup the scope to trig on the CS and set the time base so that it is possible to see the level shift clearly, to check for a reflection. The probe is moved to each of the address lines on the DUT. The start cycle and end cycle are shown in fig.5 and fig. 6 respectively. It is obvious from the figures that the address line A0 is not affected by the chip select (CS) and data line (DS). This is a good indication of signal integrity.

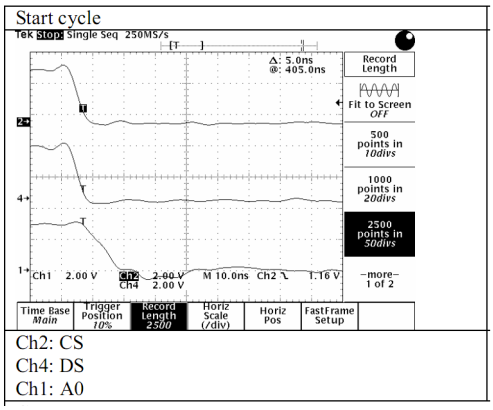

Fig. 5. Start cycle of address line A0

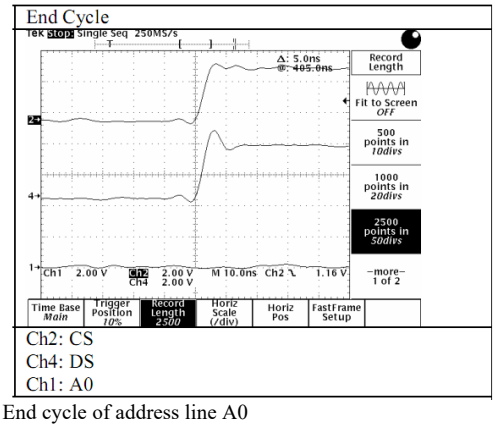

Fig. 6. End cycle of address line A0

4. Conclusion

A simple concept of Signal Integrity (SI) test is proposed by considering a backplane of some SDH products and measuring the noise immunity, pulse shape and start cycle and end cycle of different signal routed through the back plane. The concept can be extended to any electronic system design.

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