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Power Loss Analysis in 15 Level Asymmetric Reduced Switch Inverter using PLECS Thermal Models

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Abstract

The allowable power loss is the most important metrical in the research of power converters and has a significant effect on economic and technological evaluations. Two switching modulation techniques for switching angle optimization and power loss analysis in asymmetric multilevel inverter namely Phase Disposition (PD-multi carrier - based pulse width modulation at high switching frequency) and Selective Harmonic Elimination Pulse Width Modulation (SHEPWM-fundamental switching frequency). A thermal model is developed for IGBTs in the inverter using PLECS for analyzing the power losses. The power losses are computed for a 15-level asymmetric reduced switch inverter through PD switching and SHEPWM switching methods. This research proved that the power losses (Switching & Conduction losses) are less with SHEPWM switching compared to PD switching.

Keywords: Switching Losses, Conduction Losses, Power Losses, Optimized Inverter, Low Switching frequency

1. Introduction

With medium voltage and high-power levels, the usage of multilevel inverters has been more essential in previous decades. Various power semiconductor switch combinations can aid in the creation of a variety of multilevel inverter topologies for a variety of applications [1],[2]. In different implementations, various works on literature report effective use of different topologies. However, the reduced switch asymmetric topologies has drawn the most critics, out of three simple setups of NPC, DC and CHB, owing to its remarkable features [3], such as flexible construction, fast control and function, suited to different modulation techniques. Researchers mainly focused on reducing the number of switches & electronic components in MLI design for reducing the switching losses and conduction losses with minimum number of commutations [4]. These reduced switch topologies use two circuits interconnected namely, level generation circuit and polarity generation circuit [5]. The level generation circuits are energized with isolated DC sources and the polarity generation circuits reverse the sign of voltage and current waveforms of level generation circuits is presented in figure 1.

Each basic cell of proposed inverter is provided with a separate DC supply, the current on each cell is different from the load or source current on every power semi-conductor switch of a given cell. The action of power semiconductor switches is also crucially studied, and power losses are investigated. Power loss is perhaps the most critical aspect in the power system study and the economic and technological evaluations are measured accordingly [6]. The power losses of a power converter include switching losses, conduction losses, ON and OFF state losses, gate driver losses. Even so, during off state, the semiconductors switches had negligibly small leakage current, hence off state losses and gate driver losses are neglected in IGBTs. Thus, it is only appropriate to consider switching losses and conduction losses [7]. The analysis power losses on multi-level inverters are quite complex. The control of power quality and the methods of modulation to mitigate power loss is equally significant. Many researchers recommended methods based on the SPWM to reduce harmonics and evaluate the overall power loss in multilevel inverters [8]. But since SPWM has a high switching frequency, there are also high-power losses. It is therefore necessary to optimize the switching frequency for reducing power loss while mitigating THD [9]. Few approaches including optimization of switching angles to provide gating pulse for various multi-level inverter switches are proposed to further minimize power losses (4% of power delivered to the load) to a larger degree as the switching frequency is substantially decreased [10].

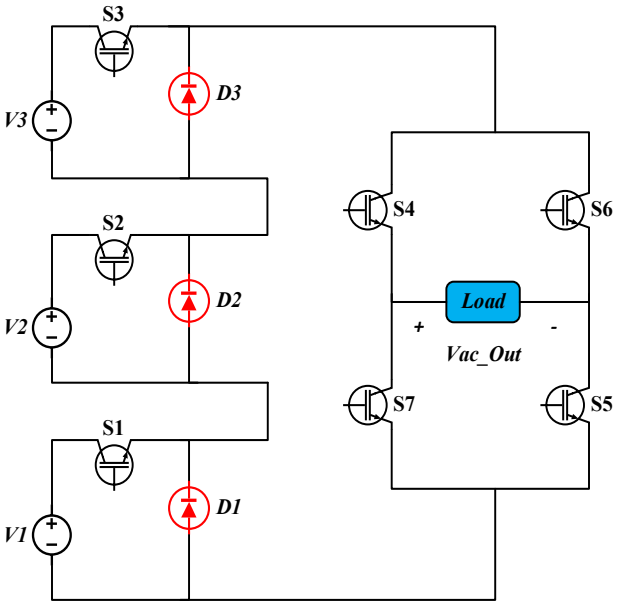

Fig. 1. An Asymmetric 15-level reduced switch inverter topology

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This article presented the thermal analysis of IGBTs of proposed inverter for switching and conduction loss calculation using PDPWM and SHEPWM on PLECS software [11]. Further the simplified models are developed for each switch of the proposed inverter on SIMULINK. The suggested simplified models evaluate the switching and conduction losses using curve fitting method from the data sheet of the IGBT using SHEPWM [12], [13], [14]. The comparative analysis of power losses obtained from PLECS thermal analysis and SIMULINK simplified models is the intended part of this research.

2. Switching control methodology of proposed inverter

In multi-level inverters, several modulation approaches have been employed to regulate the output of the voltage waveform. The switching frequency of these control systems is generally used to classify them as low or high frequency switching approaches. High frequency switching modulations are such as Sine pulse width modulation (SPWM), multi carrier based modulation schemes like Phase Disposition (PDPWM), Phase opposition & disposition (PODPWM) Alternate phase opposition & disposition (APODPWM) etc., [15] in which the active switch can trigger several times in a cycle. Whereas Space Vector (SVPWM) [16] and Selective Harmonic Elimination (SHEPWM) [17] are low frequency switching techniques in which the active power switch is triggered only one or two times in a single cycle.

In this study, both high & low frequency switching methods are implemented on proposed 15-level inverter. For the better results, the Phase Disposition PWM (PDPWM) from high frequency switching and Selective Harmonic Elimination (SHEPWM) methods was proposed to control the inverter. The SHEPWM strategy had lower switching losses and less EMI due to its low switching frequency. Furthermore, the dominant low order harmonic can be eliminated and thus the required filter size at inverter output can be optimized. In both the switching methods, the power losses are calculated, and comparative analysis is the intended part of this research.

2.1 Phase Disposition Switching method (High frequency Switching)

All the carrier signals are in-phase and level shifted in PDPWM switching pulse generation method as shown in figure (2). The single-phase reference or modulating signal is 'V' and the carrier signals are C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13 and C14. The control signal to be provided to the corresponding phase leg switches is produced by comparison of these fourteen carrier signals with the corresponding modulating signal.

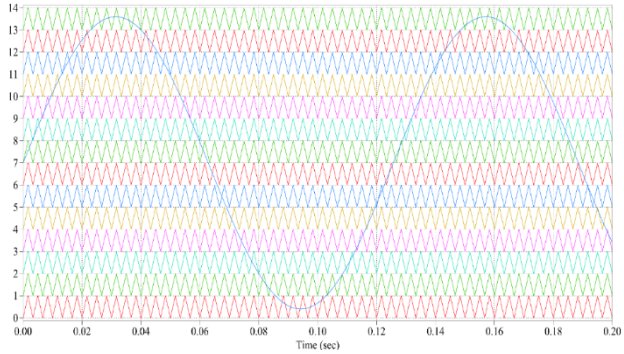


Fig. 2. Phase disposition modulation

2.2 Selective Harmonic Elimination Switching (Low frequency Switching)

SHE employs predefined switching angles and removes dominating lower order harmonics to provide the required multilevel fundamental voltage, lowering total harmonic distortion (THD).The switching angles are pre-calculated off-line and thus this is called an open loop control technique. Figure (3) shows the 15-level MLI voltage waveform. It is obvious that there are 7 switching angles that can be pre-calculated in this scenario.

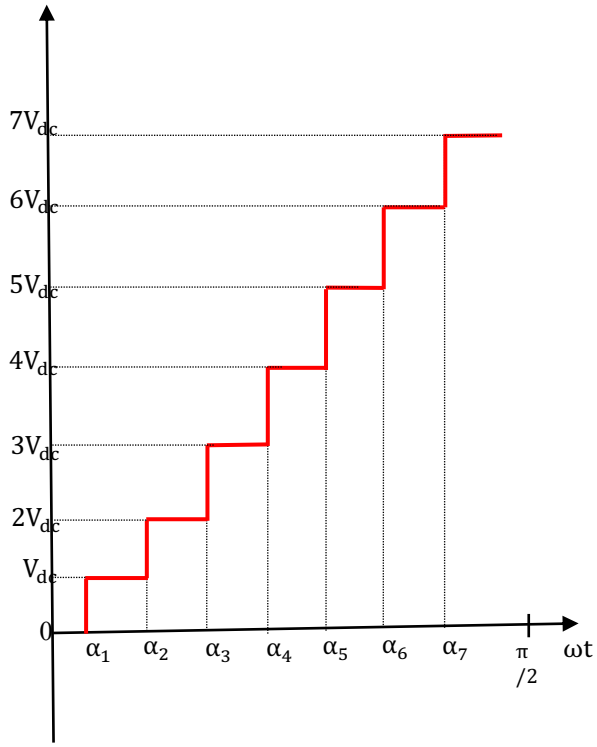


Fig. 3. Quarter wave approximation of 15-level output of multilevel inverter

The stepped voltage wave form can be expressed in the sum of periodic sine and cosine signals and a constant by applying Fourier 's expansion. The signal is made up of odd and even harmonics. The even harmonics and a dc constant are canceled due to the symmetry of the waveform quarter. Therefore, we consider only odd harmonics. All the triplen harmonics are zero for balanced three-phase systems. The output voltage waveform can usually be written as:

$$v(\omega t) = \frac{4V_{dc}}{\pi}\left\{(\cos\alpha_1 + \cos\alpha_2 + \cos n\alpha_3 + \cdots\ldots\ldots)\sin\omega t + (\cos 3\alpha_1 + \cos 3\alpha_2 + 2\cos 3\alpha_3 + \cdots\ldots\ldots)\frac{\sin 3\omega t}{3} + (\cos 5\alpha_1 + 2\cos 5\alpha_2 + 2\cos 5\alpha_3 + \cdots\ldots\ldots)\frac{\sin 5\omega t}{5} + \cdots\ldots\right\} \quad (1)$$

From figure (2) it is clear that the switching angles α_1 to α_7 must not exceed the $\frac{\pi}{2}$, therefore the switching angles should satisfy the constraint in equation (2)

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \quad (2)$$

For the proposed 15-level inverter the possible harmonics

can be eliminated are 5th, 7th,11th, 13th,17th,19th harmonics. To eliminate these harmonics, the nonlinear transcendental equations with seven switching angles are required to formulate using Selective Harmonic Elimination PWM as shown in equation (3).

$$\left.\begin{aligned}
\frac{4V_{dc}}{\pi}\left[\cos\alpha_1+\cos\alpha_2+\cos\alpha_3+\cos\alpha_4+\cos\alpha_5+\cos\alpha_6+\cos\alpha_7\right]&=f_1(\alpha)=M\\
\frac{4V_{dc}}{5\pi}\left[\cos5\alpha_1+\cos5\alpha_2+\cos5\alpha_3+\cos5\alpha_4+\cos5\alpha_5+\cos5\alpha_6+\cos5\alpha_7\right]&=f_2(\alpha)=0\\
\frac{4V_{dc}}{7\pi}\left[\cos7\alpha_1+\cos7\alpha_2+\cos7\alpha_3+\cos7\alpha_4+\cos7\alpha_5+\cos7\alpha_6+\cos7\alpha_7\right]&=f_3(\alpha)=0\\
\frac{4V_{dc}}{11\pi}\left[\cos11\alpha_1+\cos11\alpha_2+\cos11\alpha_3+\cos11\alpha_4+\cos11\alpha_5+\cos11\alpha_6+\cos11\alpha_7\right]&=f_4(\alpha)=0\\
\frac{4V_{dc}}{13\pi}\left[\cos13\alpha_1+\cos13\alpha_2+\cos11\alpha_3+\cos13\alpha_4+\cos13\alpha_5+\cos13\alpha_6+\cos13\alpha_7\right]&=f_5(\alpha)=0\\
\frac{4V_{dc}}{17\pi}\left[\cos17\alpha_1+\cos17\alpha_2+\cos17\alpha_3+\cos17\alpha_4+\cos17\alpha_5+\cos17\alpha_6+\cos17\alpha_7\right]&=f_6(\alpha)=0\\
\frac{4V_{dc}}{19\pi}\left[\cos19\alpha_1+\cos19\alpha_2+\cos19\alpha_3+\cos19\alpha_4+\cos19\alpha_5+\cos19\alpha_6+\cos19\alpha_7\right]&=f_7(\alpha)=0
\end{aligned}\right\} \quad (3)$$

Where M is the modulation index and can be defined as, Modulation index,

$$M=\frac{V_1}{V_{1max}} \quad (4)$$

Where, V_{1max} = maximum obtainable fundamental voltage.

$$V_{1max}=\frac{4kV_{dc}}{\pi}$$

V_1 = Actual fundamental voltage.
K = Degree of freedom = $\frac{L-1}{2}$
L= Levels of output voltage

Generally, Newton-Raphson 's iterative approach was applied to solve such a scheme. The big challenge is that it becomes harder to get to the solution as the number of levels gets higher. Furthermore, good initial estimated values of the switching angles are expected. The Genetic Algorithm (GA) was applied in this paper to solve the transcendental equation (3) [10]. The objective function is to minimize the total harmonic distortion (THD) with minimization limits set to be transcendental equations (2-3). It would result in the minimization of the 5th, 7th, 9th, 11th, 13th, 17th and 19th harmonics. Using the GA toolbox in MATLAB, the optimum switching angles of the 15-level proposed MLI under analysis at 0.9 modulation index were found to be 5.6^0, 10.9^0, 18.6^0, 26.5^0, 34.8^0, 44.6^0 and 61.2^0 respectively.

3. Power loss models for the proposed inverter

While using power semiconductor devices in the design of power converters there are primarily 4-types power losses will occur in the devices during the operation. These types are including: (1) Switching losses (2) Conduction losses (3) Gate driver losses. (4) OFF state losses. Gate driver losses and OFF state losses are very small and generally neglected. Hence the focus is to estimate the switching and conduction losses of the inverter.

3.1 Power losses in IGBT

The power losses in the ideal switch are negligible, while the static (conducting) and dynamic (switching) losses in the practical switch have been recorded over the switching cycle shown in Figure 4.

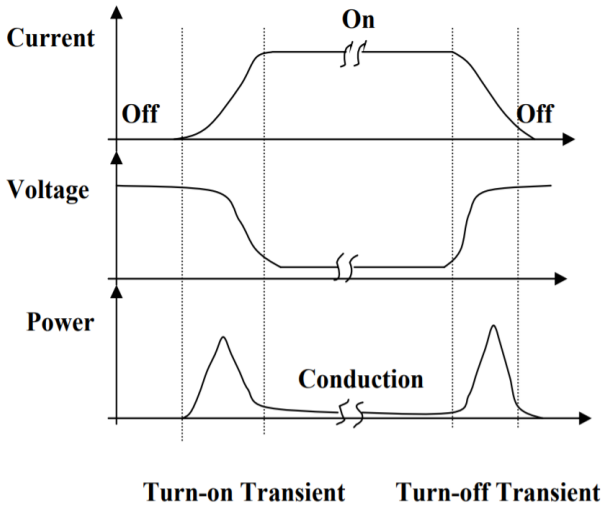


Fig. 4. Switching cycle representation of IGBT over a cycle

During the turn-on and turn-off operation of the semiconductor switch, there would be a switching time of several microseconds and the device absorbs some power when the voltage and currents are non-zero. There is a certain on-state voltage drop on the device (several volts for IGBT) while the switch is in conduction, which results in power (conduction) losses.

Power loss in the IGBT limits its use and thus becomes an important problem that cannot be ignored while designing power inverters because it influences the efficiency of the inverter. Power losses act as a heat source inside the semiconductor switch, and this heat will raise the junction temperature and increase the temperature profile inside the device. This is considered a self-heating effect which is more significant when the device is tightly packed.

To prevent destruction and severe damage to the system, the T_j junction temperature must be retained to the healthy T_{jmax} operating value typically defined by the manufacturer. Better configuration provided if the temperature gradient can be correctly predicted within the device under actual operating conditions. Thermal analysis is therefore a critical problem in the design of power converters for optimal stability, performance, and optimization of package design.

3.2 Datasheet specifications and thermal characteristics of IGBT

The IGBTs in the proposed 15-level inverter are chosen form Infineon manufacturer, the device model and specifications are given in table 1.

Table 1. Datasheet specifications of IGBT

IGBT Model	**IGA30N60H3**
Make	**Infineon**
Collector- Emitter Voltage VCEO Max	**600V**
Continuous Collector Current at 25^0 C	**18A**
Continuous Collector Current **Ic Max**	**11A**
Pd - Power Dissipation	**43W**
Device temperature	**25^0 to 175^0 C**
Gate-Emitter Leakage Current	**100nA**
Maximum blocking voltage	**400V**
Device ON state current	**120A at 175^0 C**

The IGBT device should also provide with pre-calculated conduction energy losses, turn-on losses and turn-off losses at two different temperatures of 25^0 and 175^0 for base values of on-state voltage V_{on} and conduction i_{on} current as shown in figure (5).

3.3 Thermal Simulation: Accounting for Switching and Conduction Losses

The thermal operation of electronic power systems is an important aspect, which becomes more important as the demands for portable packaging and greater power density. PLECS requires an early integration of the thermal system with the electrical design and provides a cooling method that is appropriate for each specific use. Furthermore, calculations of switching and conduction loss are quickly carried out. During loss simulations the speed of simulation is not adversely affected as ideal switching is preserved.

PLECS records semiconductor material operating conditions (forward current, voltage blocking, junction temperature) before and after any switching operation rather than evaluating semiconductor switching losses from current and voltage transients. The resulting dissipated energy is then read from a 3D look-up table using these parameters. The dissipated power is determined from the current and temperature of the device during the operation.

This synthesis of optimal switching models and accurate loss data presents an inexpensive and precise alternative to detailed device simulation. PLECS 'integrated visual editor is used to access the appropriate datasets.

3.4 Thermal modelling of IGBT using PLECS

PLECS is a software tool that has been developed by Plexim to perform the system level simulation of electric circuits, particularly intended for power electronics but can be used for all power systems. Apart from the electrical system, PLECS includes the ability to model controls and various physical domains such as thermal, magnetic and mechanical systems.

For IGBT, PLECS uses only one of its dc characteristics, the high-valve output of a control signal that is linearly interpolated according to the user points. With the dynamic properties of this IGBT, it is important especially to accurately model the dependencies of the entire energy from switching E_{ts} on several variables, such as T_j, the current collector I_C, R_G, or overvoltage switching. These relationships can be used in PLECS and they are often interpolated linearly, as with the dc characteristics. The system also makes the reliance on the value entered by the user for switching energy losses. The energy values of the on and off losses are entered independently, both for the IGBT and for the reverse diode.

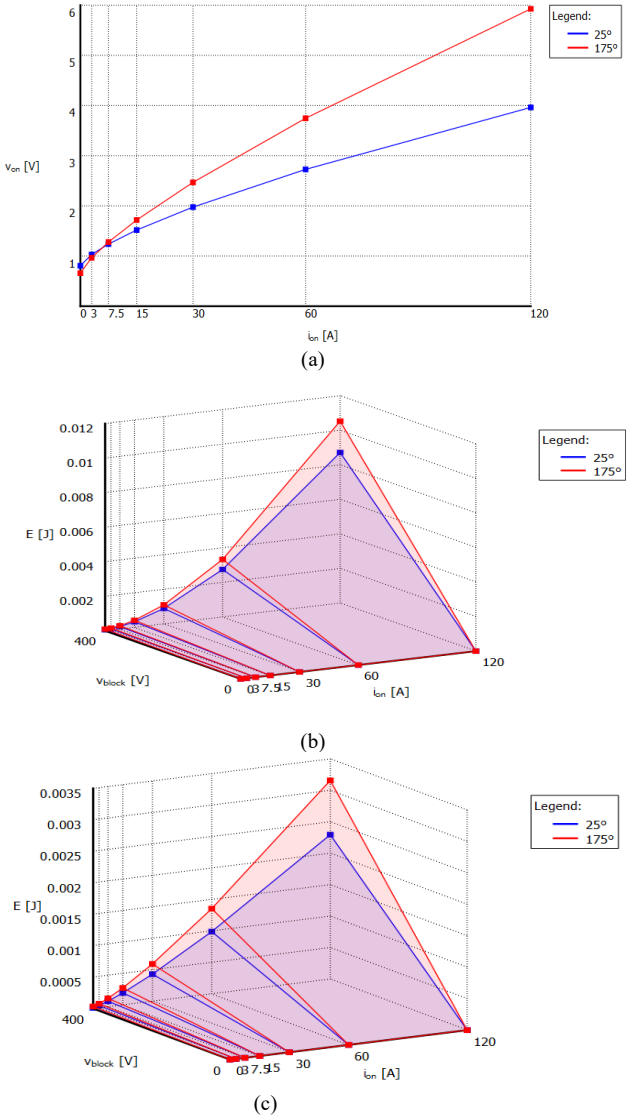


Fig. 5. Thermal characteristics of IGBT from look-up tables (a) Conduction losses (b) turn_ON losses (c) Turn_OFF Losses

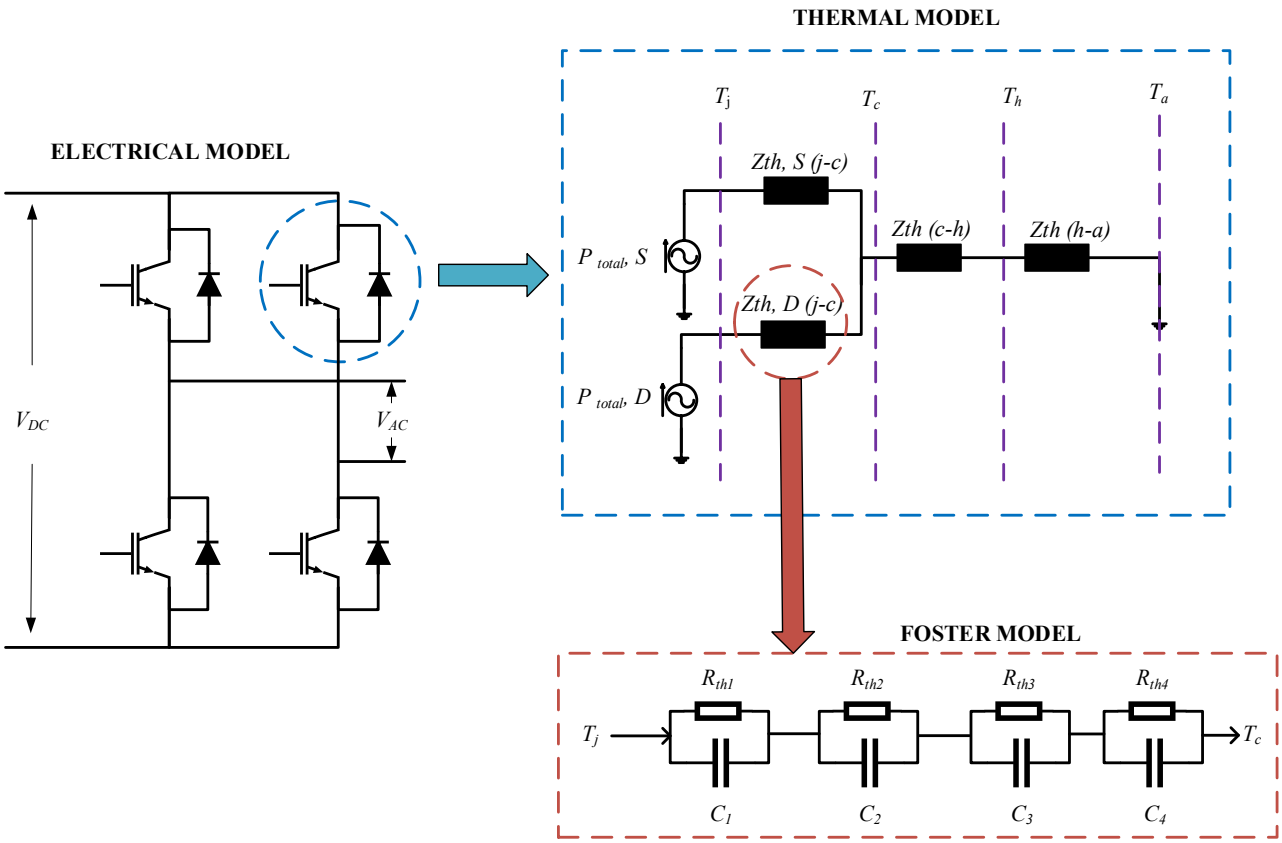


Fig. 6. Power loss calculation for proposed 15-level inverter using thermal analysis of IGBTs in PLECS

The thermal model of IGBT is shown in figure (6), which is modelled for one of the IGBT switch of auxilliary circuit of proposed 15-level inverter. The impedence of the thermal model is designed from foster circuit model for junction temparature to case temparature. Considering junction temparature as 150^0 C and thermal impedance of 1.25Ω the foster thermal model is designed on PLECS for 15-level inverter. All the 7- IGBT switches are modelled thermally using heat sink in PLECS simulation for power loss analysis. Both the conduction losses and switching losses are measured using this analysis for both PDPWM (high frequency switching) switching and SHEPWM switching (low frequency switching).

3.4 Concept of heat sink

The heatsink absorbs the switching and conduction losses of all devices inits boundary. A heat sink simultaneously describe an isothermal atmosphere and distribute its temperature to the surrounding components. The semi conductors mounted on the heat sink will have same case temparature. The witching energy losses are modelled as direct type pulses on PLECS, having zero width and infinite height. Thus either the thermal capacitance of the thermal sink needs to be specified or a thermal chain with a capacitance should be used, in order to avoid the infinite thermal resistance to switching energy pulses.

3.5 Calculation of total cycle-average losses

The total power dissipation of each semiconductor is also a factor of interest. The average losses for a device can be determined by adding the losses in the next switching period to the average power pulse. The average cycle method of loss calculation is shown in figure 8. The C-Script PLECS Block is used to perform integrated loop summing on energy loss operations [18].

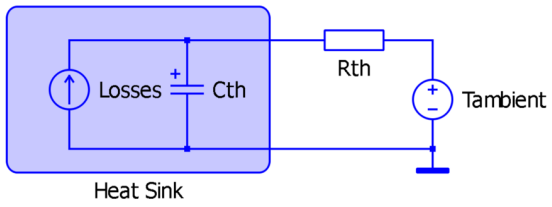


Fig. 7. Electrical equivalent of thermal citcuit

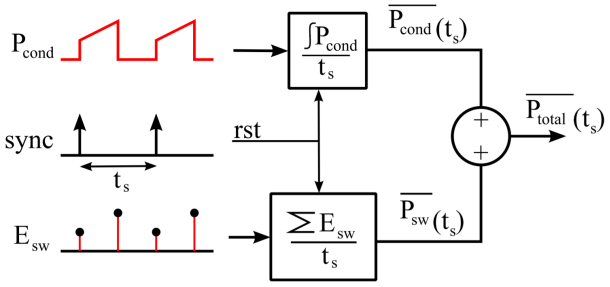


Fig. 8. Calculation of total cycle-average losses

4. Results and Discussions

4.1 Power loss analysis using PLECS thermal modelling

The switching and conduction losses for both high and low switchng frequency controls were plotted using PLECS simulation. The switch wise device temparature, conduction losses and switching losses are plotted in figure. 12 for PDPWM switching. The IGBT swithes 'S_1', 'S_2' and 'S_3' are a high frequency switches in the operation of the proposed inverter hence it undergoes for on and off for sevral times resulting more switching losses. Similarly the switches 'S4', 'S5', 'S6' and 'S7' are the low frequency switches, which has low power losses. The power losses calculated from both PDPWM and SHEPWM using PLECS simulation are tabulated in table 2 for each IGBT switch of the 15-level inverter.

Table 2. Power losses & THD with Phase Disposition (High Frequency switching)

Switches	High Frequency Switching (PDPWM)			Low Frequency Switching (SHEPWM)		
	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)
S1	4.6019	0.0155	4.6174	4.0303	0.0091	4.0394
S2	5.4398	0.0129	5.4527	4.4049	0.0077	4.4126
S3	7.135	0.008	7.143	5.1532	0.0049	5.1581
S4	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S5	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S6	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S7	4.5187	0.002	4.5207	3.0227	0.0002	3.0229

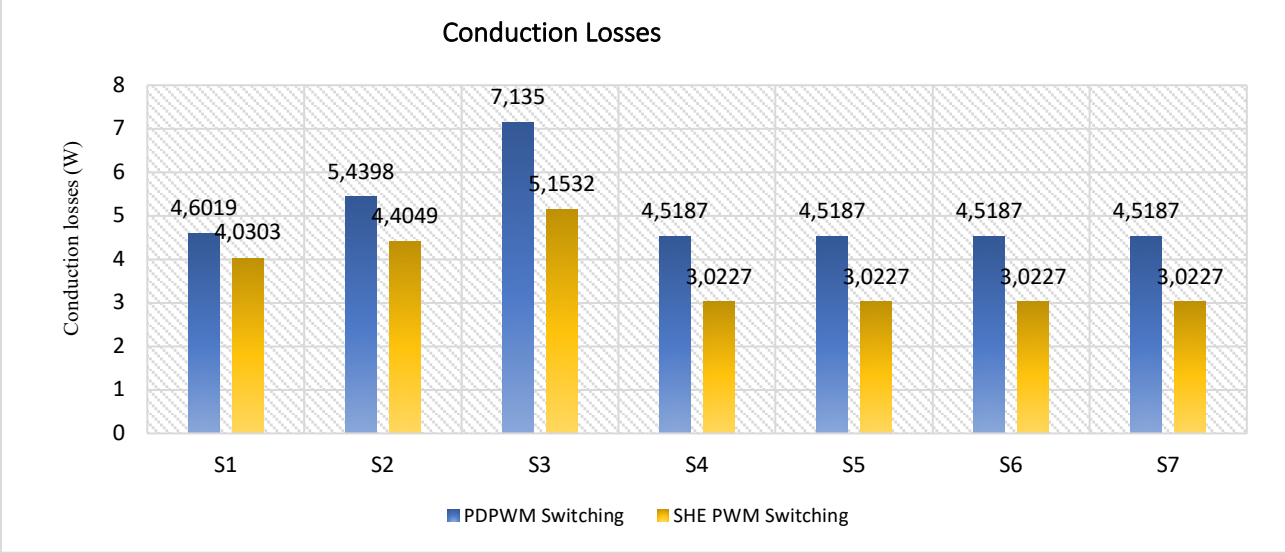


Fig. 9. Conduction losses comparison with High & Low switching frequency

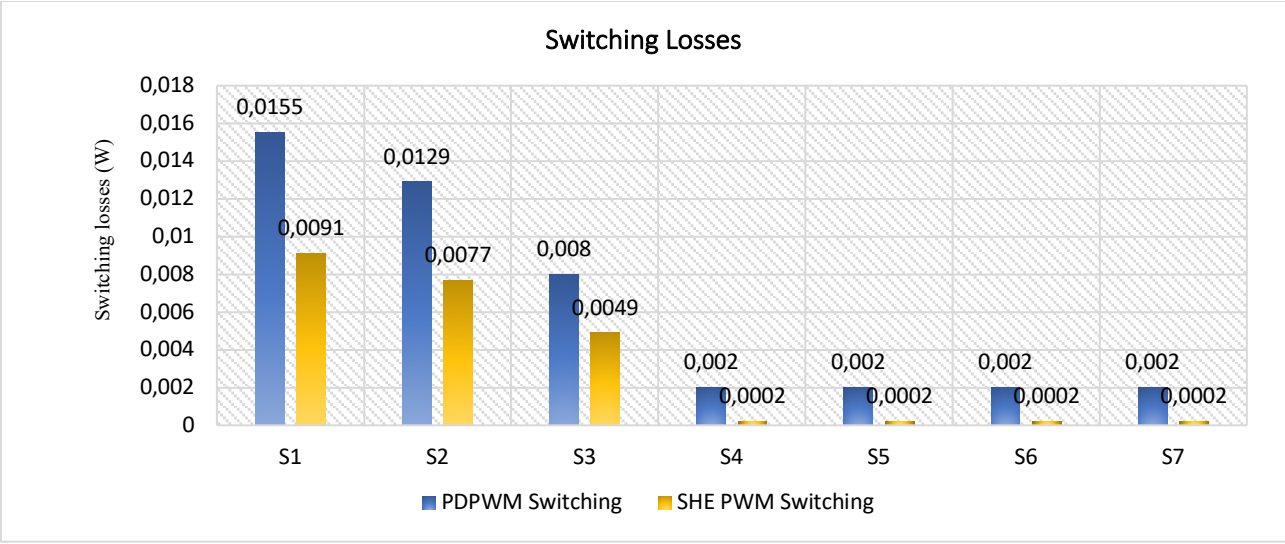


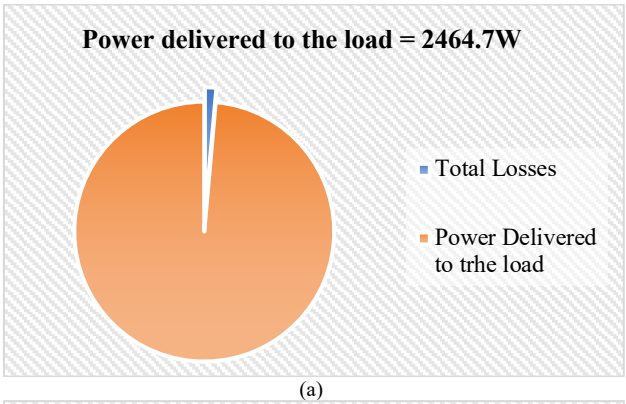
Fig. 10. Switching losses comparison with High & Low switching frequency

The comparative analysis of conduction losses with high and low switching frequency control methods are given in figure.9. Here SHEPWM switching gives the less conduction losses than the PDPWM. Also, the switching loss comparison analysis is given in figure. 10 and observed that the switching losses are comparatively low in SHEPWM switching method than PDPWM.

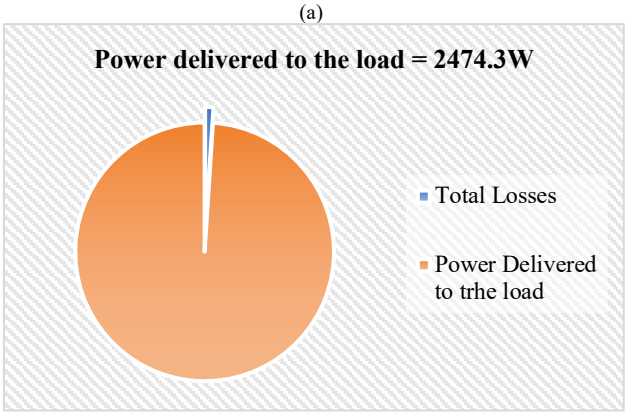
The proposed inverter input power rating is 2500W at

259V and 9.65A of input current. The total power loss measured from high switching frequency method is 35.3W. Therefore, the power delivered to the load for high switching frequency control is 2464.7W, which gives the efficiency 98.59% as shown in figures (11a and 11c). The total power loss measured by low switching frequency control is about 25.7W. The power delivered to the load in this control method is 2474.3W, which gives the efficiency of 98.97% as shown in figures (11b and 11d).

The SIMULINK model presented in figure 11 has been run for different modulation index and corresponding power losses and THD is tabulated in table 3. The results show that 0.9 modulation index the THD is minimum of 5.75% and the power losses are 26.04W. The variation of power losses with modulation index in plotted in figure 19.



(a)



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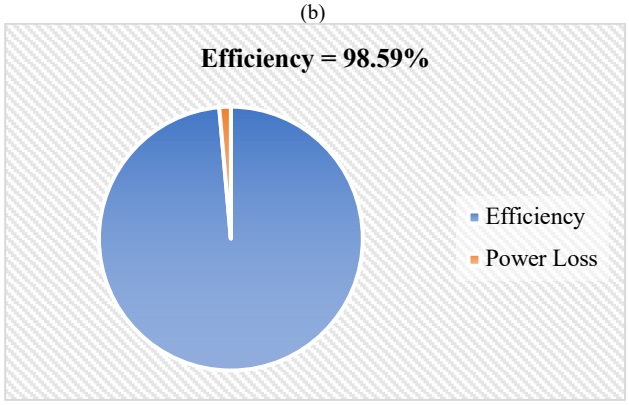

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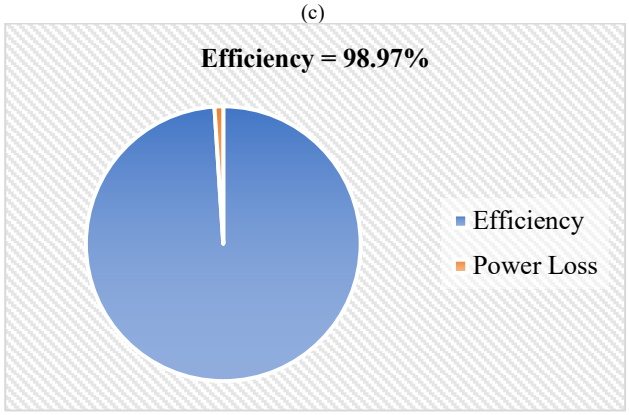

(d)

Fig. 11. Power Loss Analysis using PLECS thermal modelling (a) High switching frequency (b) Low switching frequency (c) Efficiency with High switching frequency (d) Efficiency with Low switching frequency.

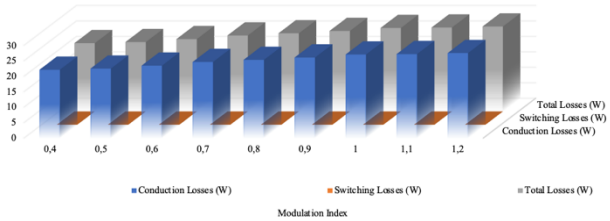

Fig. 12. Power Losses Vs Modulation index

Table 3. Power loss & THD variation with modulation index by SHEPWM control

Modulation Index	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)	THD %	Fundamental Voltage
0.4	22.062	0.0248	22.0868	6.88	209.27
0.5	22.423	0.0242	22.4472	6.59	220.23
0.6	23.382	0.0236	23.4056	6.32	232.56
0.7	24.561	0.0235	24.5845	5.99	234.26
0.8	25.257	0.0231	25.2801	5.86	240.92
0.9	26.016	0.0229	26.0389	5.75	245.61
1.0	26.984	0.0216	27.0056	5.78	252.72
1.1	27.125	0.0214	27.1464	5.61	258.45
1.2	27.459	0.0217	27.4807	5.73	258.06

6. Conclusions

Semiconductor device transient losses have a major influence on the performance of the power converter circuit in which they are employed. A 15-level asymmetric inverter is designed and implemented with reduced no of switches suitable for PV applications. The performance of this asymmetric inverter can be analysed based on the total harmonic distortion and power losses. It is extremely crucial to analyse losses in multi-level inverters as accurately as possible. Conduction and switching losses are among the most common types of losses in multi-level inverters. The switching and conduction losses are evaluated separately considering junction temparature as 150^0 C and thermal impedance of 1.25Ω the foster thermal model is designed on PLECS for 15-level inverter and corresponding plotes were plotted for high frequency switching (PDPWM) and low

frequency switching (SHEPWM). The efficiency of the inverter at 0.9 modulation index is proved 98.59% with PDPWM and 98.97% using SHEPWM. The overall inverter losses were found to constitute around 1.004% of the total power delivered by the inverter at low switching control with the inverter efficiency of 98.97%. It is concluded that the efficicency of the proposed inverter is approximately same as 98.97% using PLECS thermal model at low switching frequency control method.

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