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Discrete Control of Quadratic Converter for Solid State LED Driving Applications

Yadlapalli Ravindranath Tagore[1,*], Kotapati Anuradha[2] and Koritala Chandra Sekhar[1]

[1]*RVR & JC College of Engineering, Electrical and Electronics Engineering Department, Chowdavaram, Guntur, Andhra Pradesh, India-522 019*
[2]*Vallurupalli Nageswara Rao, Vignana Jyothi Institute of Engineering & Technology, Electrical and Electronics Engineering Department, Hyderabad, Telangana State, India-500 090*

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Abstract

Nowadays LEDs have a prominent role for realizing energy saving all over the world. Moreover, there is a need to design efficient LED drivers following the present technological advancements of the LED lighting systems. The main objective is associated with the excellent current regulation of the LED driver. Therefore, this paper exaggerates the performance achievements of the quadratic buck converter (QBC) for driving LEDs. At first the converter modeling is fufiled based on the eminent state space time averaging approach and the essential control loop transfer functions are attained. The stable operation of QBC is accomplished based on the digital and analog based current control strategies. The PSIM simulation outcomes of QBC are explored with respect to the above control strategies in terms of the steady load and line perturbations. The efficiency curves are presented at various QBC input voltages along with bar charts with respect to the losses of the QBC. Moreover, the economic considerations for the real-time implementation of the analog and digital controllers are highlighted.

Keywords: LEDs, current regulation, average current-mode control, dynamic performance.

1. Introduction

The advances in LED technology should be supported by the development of well fitted LED lamp drivers. The LED lamps have many advantages such as low power consumption, no warm-up time, highly durable, environmental friendliness and subsequent on-off cycling, presented by Bruno [1]. They are used in place of mercury vapor lamps, sodium vapor lamps, tungsten filament and CFL lamps. The LED lamps are not permitted to place them directly on the supply lines. Hence, a well-designed driver is imperative for realizing favorable LED current regulation. Several LED lamp driver dc-dc converters are addressed in the literature for various types of LEDs, emphasized by Esteki et al., Teixeira et al., Yadlapalli et al. [2-4]. The buck topology is simple as a lamp driver. However, it has the drawback of poor dimming control that leads to flickering of lamps. Importantly, the PWM controllers assign some limits at higher switching frequencies. Furthermore, the linear region operation of the converter switch results in reduced efficiency. An integrated double buck-boost (IDBB) has the advantages like good life and reduced current ripples, designed by Alonso et al. [5]. However, it has been built with more number of components. On the other hand, a very high gain is grabbed with the quadratic boost converter, proposed by Jahangiri et al. [6]. But, it necessitates the higher number of circuit components with an impact on the slight raise in the duty ratio. The major hindrance related with peak switch currents is going to limit the application of a soft switching converter, implemented by Tehrani et al. [7]. The multi-output current-source-mode converters are superior without the use of inductors, developed by Dong et al. [8]. The requirement for many outputs is severely affected by a rise in the power component number. A LED series current regulator is efficient with reduced current ripple, as analyzed by Ribas et al. [9], but its efficiency highly relies on the LED voltage besides the bus voltage. The LED driver operation is fulfilled by the Quadratic Buck Converter (QBC) with an excellent over-current protection, detailed by Elias et al. [10]. However, the presence of high LED peak-to-peak current ripple can result in more flickering phenomenon. Inspire of definite drawbacks, the average current mode control (ACMC) equipped QBC is implemented by Yadlapalli et al. [11]. The important issue is the existence of right-half-plane zeros (RHPZs) in continuous current associated QBC operation. The RHPZs are always effective in limiting the QBC control bandwidth. This downside is intolerable with voltage-mode control (VMC) based QBC. Moreover, the peak CMC is objectionable with degraded noise margin. In ACMC, the control transfer functions are derived using esteemed modeling techniques. The ACMC present the benefits namely overcurrent protection, quicker dynamics and curtailed subharmonic oscillations. Hence, this research work emphasizes the QBC design with the analog and digital ACMC. The design of the digital ACMC is succeeded in s-domain and thereafter effectuated to Z-domain based on Tustins method. The digital ACMC gives more design flexibility and parameters can be easily tuned as compared to the analog ACMC. The other prominent benefits are enhanced noise immunity, free from parameter drift, considering nonlinearities, realizing complex algorithms and more reliable. The implementation of the real-time digital controllers is based on the microcontrollers, field-programmable gate arrays (FPGAs) and digital signal processors (DSPs). In this research work, the simulation results of the analog and digital ACMC based QBC are

*E-mail address: yrtagore@gmail.com
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highlighted in terms of the steady load and line perturbations using PSIM software. The efficiency curves are presented at various QBC input voltages.

The principal objectives of this research paper are:

- To model the dc-dc converter in view of deriving the essential control transfer functions.
- To design an efficient digital ACMC based converter along with the economic considerations.
- To achieve good current regulation of the LED driver.
- To grab good converter dynamics associated with the line regulation.

This research paper is structured as given; Section 2 gives the QBC basic aspects, whereas converter modeling is detailed in Section 3. Sections 4 & 5 give the various simulation case studies and conclusions.

2. Proposed converter

The QBC schematic is illustrated in Fig. 1. The output dc and input dc voltages are shown by

$$\frac{V_o}{V_{in}} = D^2 \tag{1}$$

Where V_o & V_{in} are the output dc and input dc voltages of QBC and D is duty ratio. It has one switch, two inductors, two capacitors and three diodes. The main advantage of QBC is that it can realize high step-down conversion ratios. Different case studies are taken for the analysis of robustness against input voltage variations or load current regulation.

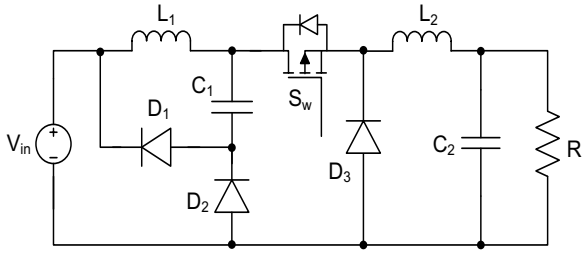


Fig. 1. Schematic of QBC [11]

3. Modeling and control strategies

The DC-DC converters can be modelled for analyzing the QBC dynamics. Many researchers have reported different modeling techniques in the literature presented by Yadlapalli et al. [11-12]. The literature highlights the very prominent modeling technique namely state-space averaging methodology. This methodology is applied for QBC for getting different control transfer functions using Eq. (2).

$$\frac{d\,\tilde{x}_i(t)}{dt} = A_{ss}\,\tilde{x}(t) + B_{ss}\,\tilde{u}_i(t) + B_{ii}\,\tilde{d}(t) \tag{2}$$

$$\tilde{y}_o(t) = C_{ss}\,\tilde{x}(t) + E_{ss}\,\tilde{u}(t) + E_{ii}\,\tilde{d}(t)$$

$$A_{ss} = A_{11}D + A_{22}(1-D)$$

$$B_{ss} = B_{11}D + B_{22}(1-D)$$

$$C_{ss} = C_{11}D + C_{22}(1-D)$$

$$E_{ss} = E_{11}D + E_{22}(1-D)$$

$$B_{ii} = (A_{11} - A_{22})X + (B_{11} - B_{22})U$$

$$E_{ii} = (C_{11} - C_{22})X + (E_{11} - E_{22})U$$

The necessary small signal transfer functions are obtained from Eq. (3).

$$\tilde{x}_s(s) = \begin{bmatrix} (SI-A)^{-1}B_{ss} & (SI-A)^{-1}B_{ii} \end{bmatrix} \begin{bmatrix} \tilde{u}_{in}(s) \\ \tilde{d}(s) \end{bmatrix} \tag{3}$$

$$\tilde{y}_o(s) = \begin{bmatrix} C_{ss}(SI-A)^{-1}B_{ss} + E_{ss} & C_{ss}(SI-A)^{-1}B_{ii} + E_{ii} \end{bmatrix} \begin{bmatrix} \tilde{u}_{in}(s) \\ \tilde{d}(s) \end{bmatrix}$$

The transfer required for controller design are $\frac{\widehat{iL_1}(s)}{\hat{d}(s)}$ and $\frac{\widehat{Vo}(s)}{\hat{d}(s)}$. These TFs are useful in the design of ACMC for LED lighting systems.

4. Simulation Results

The performance of QBC is analyzed by considering the various case studies. The QBC simulation nominal parameters are presented in the following Table 1.

Table 1. QBC nominal specifications

Nominal simulation Parameter	Value
V_{in}	311 V
Inductance (L_1)	0.165µH
Inductance (L_2)	0.180 µH
C_1=C_2	1 µF
f_{sw}	100 kHz
V_0	170 V
Load R	8.5 kΩ

Eq. (4) shows the inductor current control transfer function of QBC.

$$\frac{\tilde{i}_{l1}(s)}{\tilde{d}(s)} = \left(\frac{854700s^3 + 53499020s^2 + 789580000s + 4398763209200}{s^4 + 152897s^3 + 62984786s^2 + 5076594324s + 28570382980} \right) \tag{4}$$

Eq. (5) shows the TF of QBC for duty signal-to-output dc voltage.

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \left(\frac{29435761860s^2 - 256783245720s + 45327894364534}{s^4 + 2485718s^3 + 6773992685s^2 + 769340296574s + 2178373586565} \right) \tag{5}$$

Bode plots of the transfer functions (TFs) given in Eq. (4) and Eq. (5) are depicted by Fig. 2 and Fig. 3.

There should be a proper bandwidth relation between the two control loops. The main feature is that the inner loop provides the inherent over current protection. The two loops are designed such that the overall converter system should always be stable at all input or load variations. Different case studies are taken for the analysis of robustness against input voltage variations or load current regulation. The TFs associated with fast current and slow voltage loops compensators can be obtained in s-domain based on Eq. (4)

and Eq. (5). These TFs are realized in Z-domain based on Tustin method.

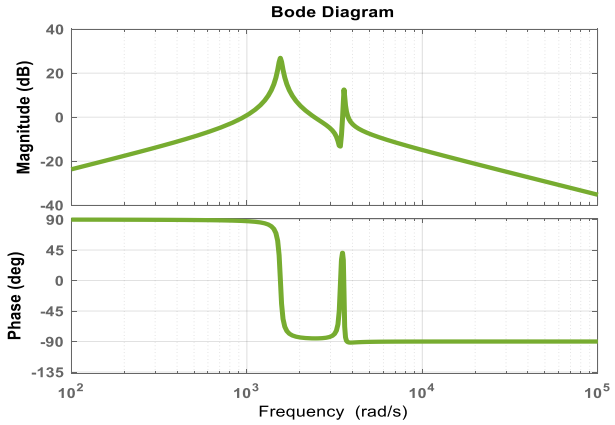


Fig. 2. Bode illustration of control duty signal-to-input side inductor current

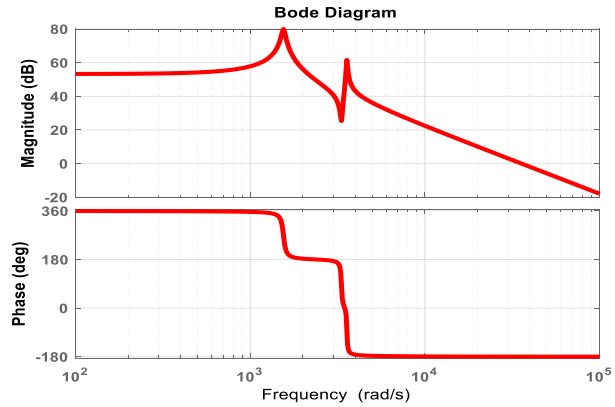


Fig. 3. Bode diagram for PWM signal-to-dc load voltage

The low pass filter TF of current feedback loop is obtained as

$$F(z)=\frac{1+Z}{(-1+3Z)} \tag{6}$$

The TF of current loop is obtained as

$$C_1(Z)=\frac{(7Z^2-0.9495Z-0.12)}{(Z^2-0.00756Z+0.4)} \tag{7}$$

The TF of voltage loop is given as

$$C_2(Z)=\frac{(2Z^2-0.00045Z-1.8)}{(Z^2-1)} \tag{8}$$

The QBC block diagram with digital-ACMC is shown in Fig. 4.

As mentioned earlier, the primary objective of this research study is to actualize superb steady and dynamic LED current regulations of the ACMC based QBC over the universal ac input voltages ranging from 90 V to 265 V (rms). This should also engender the trimmed flickering effect in order to avoid numerous human health issues such as eye strain, headache, fatigueless, blurred vision and neurological problems. Moreover, it helps to curtail the current ripple in view of ascertaining the safe operating temperatures of the LEDs. Otherwise, high operating temperatures lead to reduction in the forward voltage of the LEDs. However, as shown in Fig. 4, the inner current loop of the ACMC strategy spontaneously decreases the duty cycle without causing burning of the LED string. The following sections highlight the case studies associated with the steady and dynamic LED current regulations.

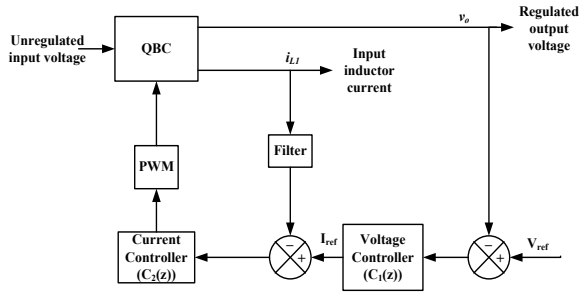
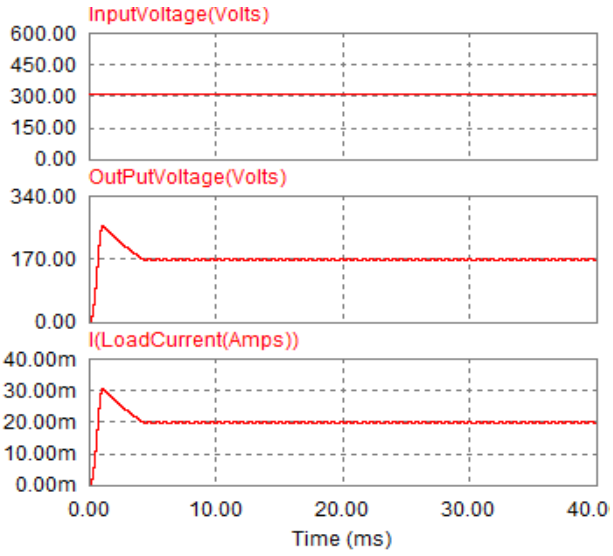


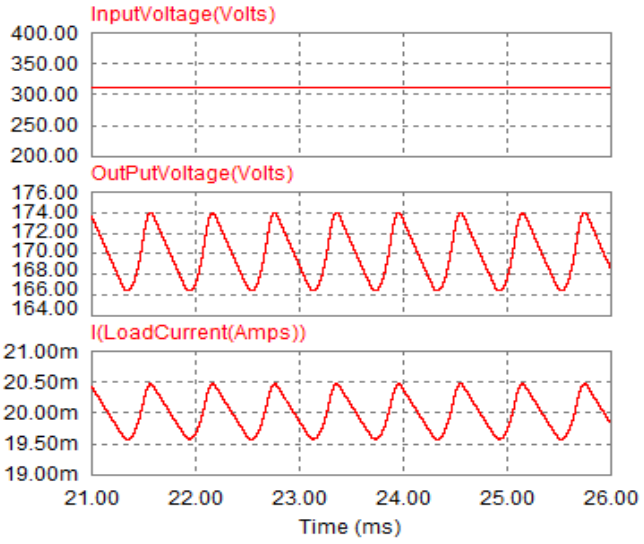
Fig. 4. Block diagram of QBC with Digital ACMC

4.1. Performance of Analog ACMC and Digital ACMC based QBC at 311 V

The analog ACMC and digital ACMC based QBC waveforms are interpreted in Fig. 5 (a) and Fig. 6 (a). At constant load current of 20 mA, the steady state current ripple is ±2.25% in case of ACMC, whereas ±0.5% with Digital ACMC, which are observed in the magnified waveforms of Fig. 5 (b) and Fig. 6 (b).

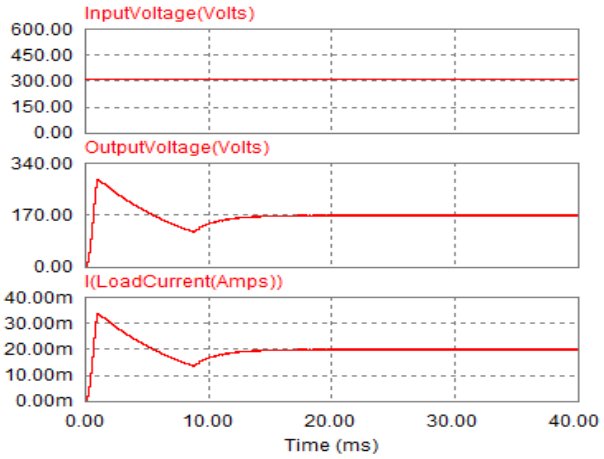


(a) Unexpanded

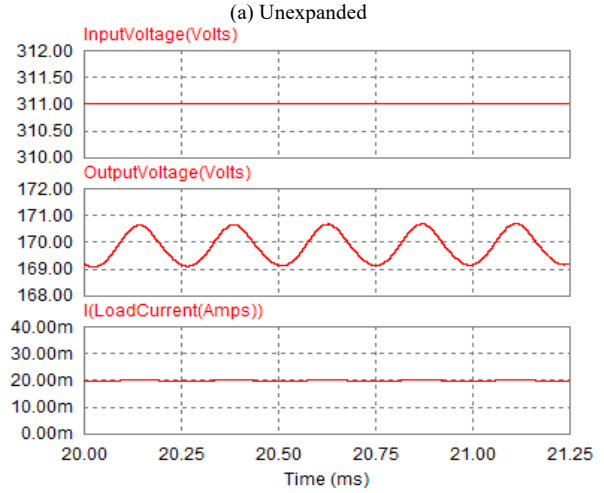


(b) Magnified

Fig. 5. QBC results for analog ACMC at constant load



(a) Unexpanded



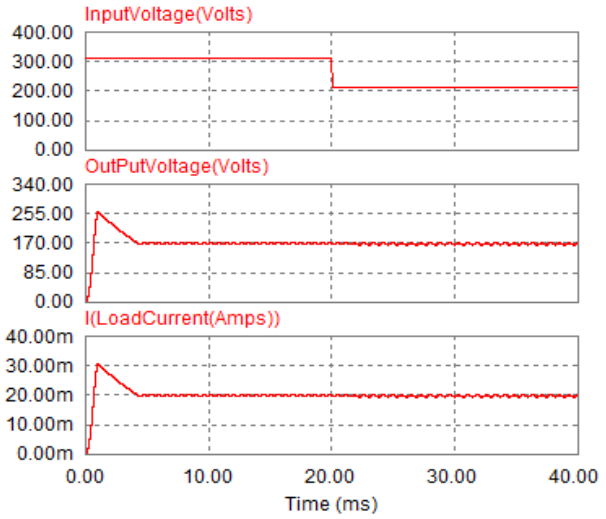
(b) Magnified

Fig. 6. QBC results with digital ACMC at constant load

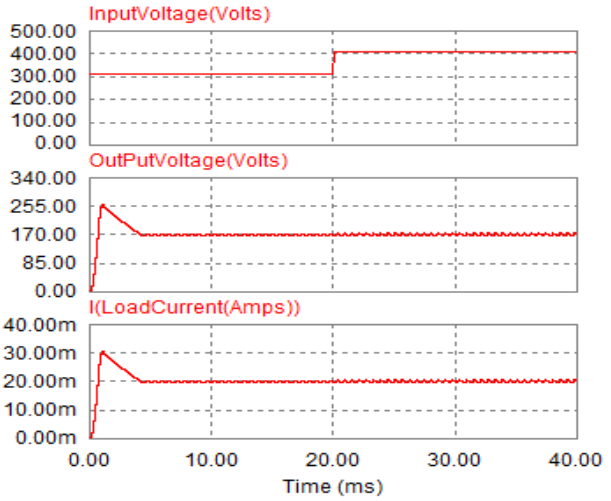
4.2. Performance of Analog ACMC and Digital ACMC based QBC for step input voltages

Figs. 7 (a) & (b) present the analog-ACMC based QBC, whereas digital-ACMC based QBC is focused in Figs. 8 (a) & (b), which considers the two distinct case studies fulfilled with sudden step input dc voltages. The digital-ACMC explores the remarkable dynamic regulation as contrasted to the analog-ACMC without any oscillations or peaks. The dynamic settling time of 1 msec is achieved in case of the digital-ACMC based QBC as contrasted to the analog-ACMC with 2 msec. Importantly the transient current dip is only 0.4 mA in the digital-ACMC based QBC as compared to the analog-ACMC based QBC with 0.58 mA.

Fig. 9 & Fig. 10 present the load current ripple comparison at different input dc voltages of 211 V and 411 V. This is due to the alterations in the ac supply voltage that leads to perturbations in the QBC input dc voltage. Table 2 and Table 3 highlight the steady state current regulation comparison of QBC with the above control strategies. The current regulation seems to be good in case of digital-ACMC as compared to the analog-ACMC. The considered dc input voltage range of QBC is from 211 V to 411 V. It implies to the same universal ac input voltage ranging from 90 V to 265 V (rms). When dc input voltage is reduced to 211 V, the duty cycle of the QBC is incremented in order to acquire the desired LED string voltage and current. At higher dc input voltage of 411 V, the duty cycle of the QBC is decremented in order to grab the desired LED string voltage and current. Importantly, the LED current ripple is identified to reside within the limits of less than ±5% and meeting the IEEE standards 1789-2015 recommendations. The reduced peak-to-peak current ripple not only ensures the diminished current stresses but also the thermal stresses of the LEDs. The LEDs will always face the safe operating temperature limits. Moreover, the flickering effect is lessen as PWM current has a frequency of more than 400 Hz. The ACMC strategy can engender the gain and phase margins as close to 6 dB and 45º.

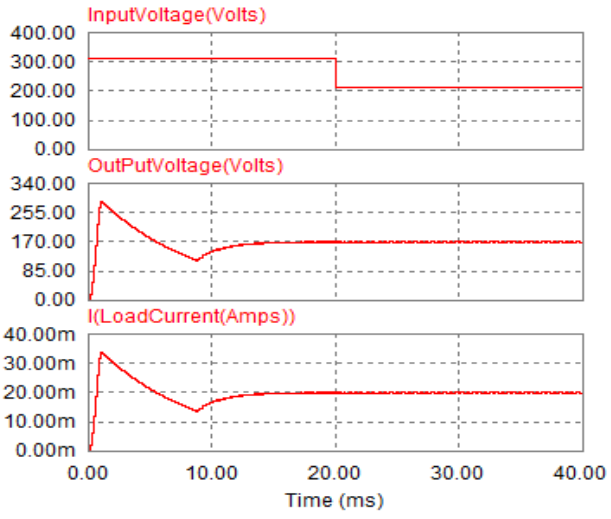


(a)

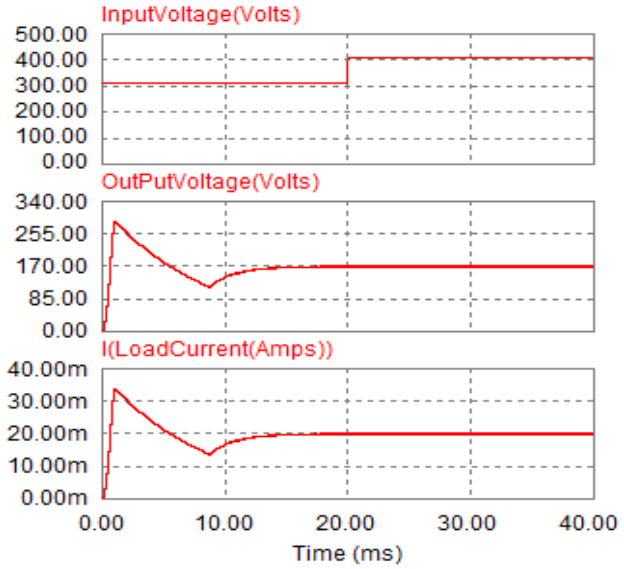


(b)

Fig. 7. QBC waveforms with analog ACMC based QBC (a) 311 V - 211 V (b) 311 V - 411 V

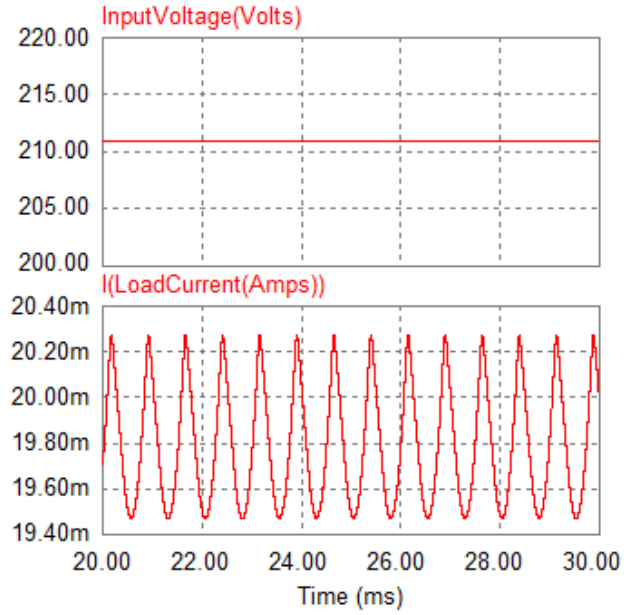


(a)

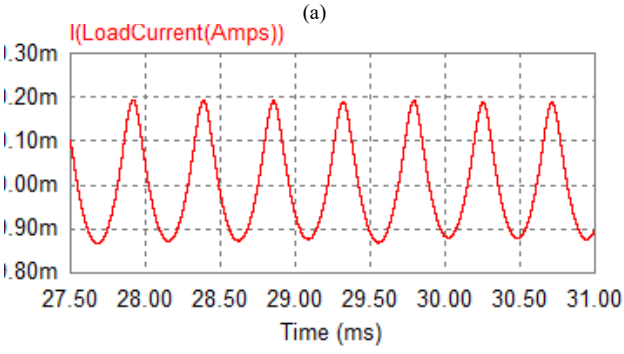


(b)

Fig. 8. QBC results with digital ACMC based QBC (a) 311 V - 211 V (b) 311 V - 411 V



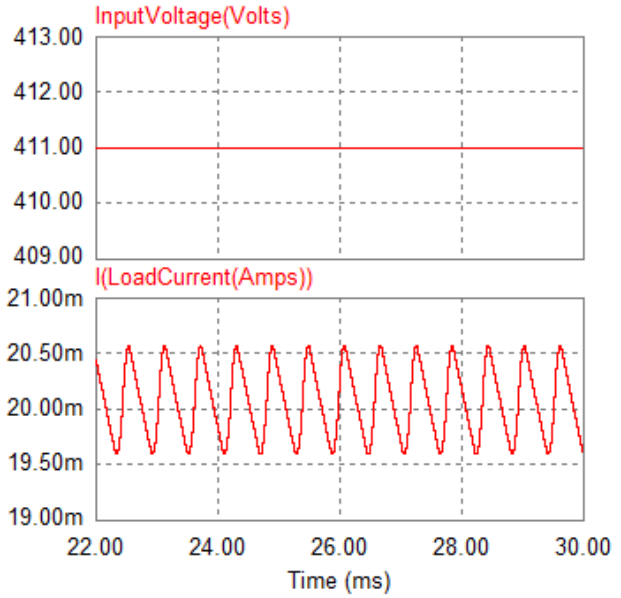
(a)



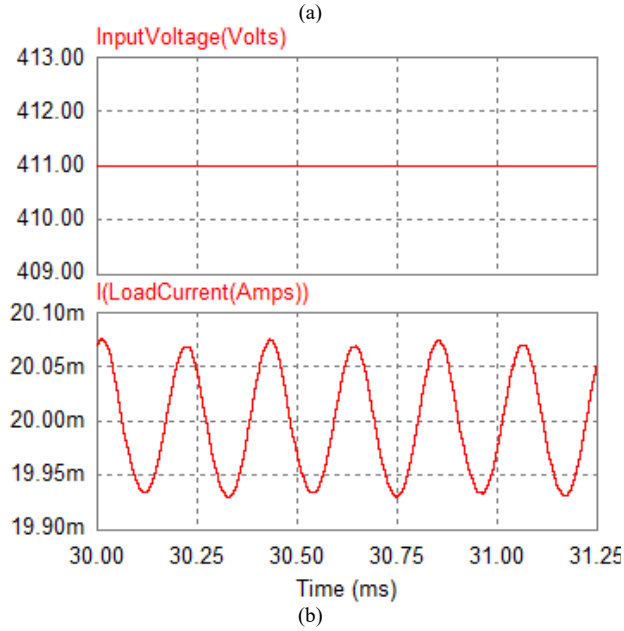
(b)

Fig. 9. Steady state ripple current comparasion at 211 V (a) Analog ACMC (b) Digital ACMC

Fig. 11 & Fig. 12 present the dynamic load current regulation comparison of QBC for the step input voltages from 311 V - 211 V and 311 V - 411V. This is due to the sudden alterations in the ac supply voltage that leads to abrupt perturbations in the QBC input dc voltage. Table 4 along with Table 5 highlight the dynamic line regulation issue comparison with the above two control strategies. The transient performance is extremely good with the digital-ACMC as compared to the analog-ACMC. In case when the dc input voltage of the QBC falls spontaneously from 311 V to 211 V, the duty cycle of the QBC is incremented dynamically in response and thereby producing the desired LED string voltage and current. When the dc input voltage of the QBC drastically increases from 311 V to 411 V, the duty cycle of the QBC is decremented dynamically and thereby enacting the desired outputs. Thus, the duty cycle of the QBC is incremented or decremented with respect to the fall or rise of the input voltage. Moreover, the LED current ripple is noticed to reside within the limits of less than ±5% and thereby meeting the IEEE standards. The simulation results almost highlight the first order response with negligible peak overshoots in the LED string voltage and current. This superior converter dynamics are due to higher bandwidth provided by the controller. It also gives robust performance not only for the supply voltage alterations but also the converter parameter variations.

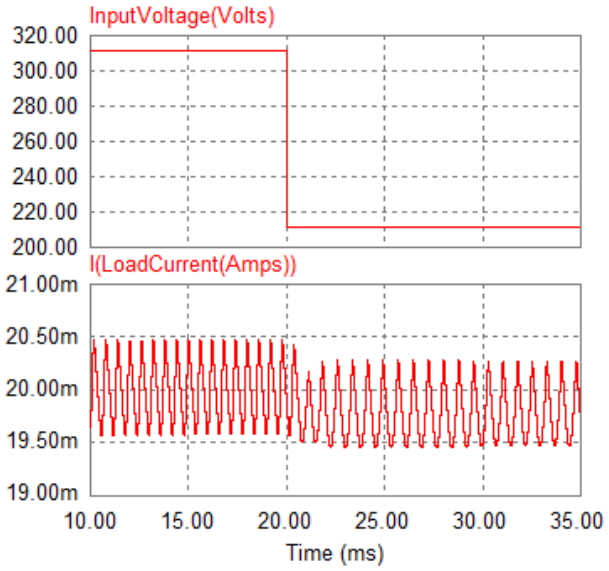


(a)

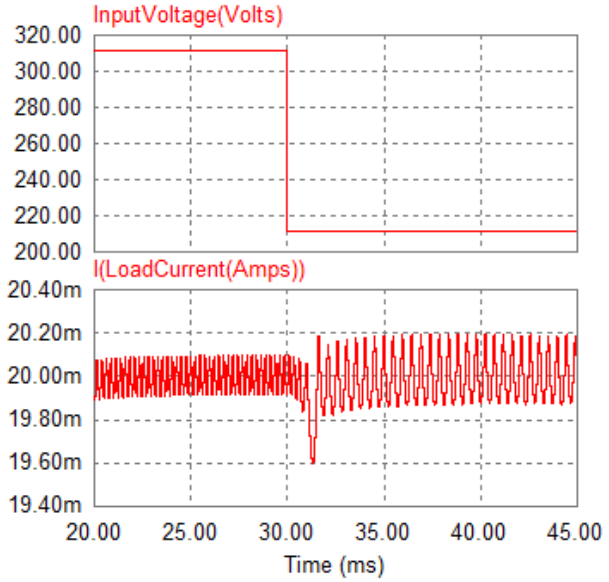


(b)

Fig. 10. Steady state ripple current comparasion at 411 V (a) Analog ACMC (b) Digital ACMC

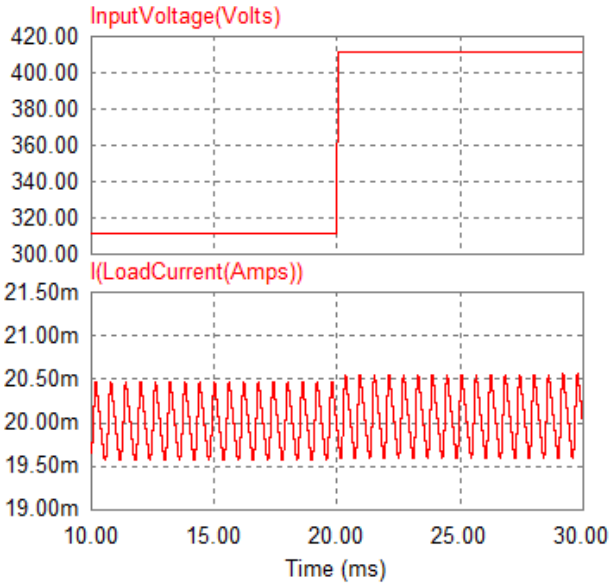


(a)

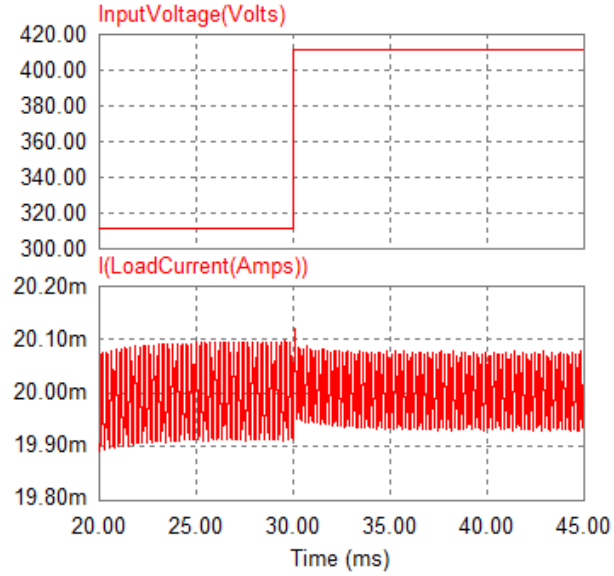


(b)

Fig. 11. Dynamic performance comparasion at 311 V - 211 V step input voltage a) Analog ACMC (b) Digital ACMC



(a)



(b)

Fig. 12. Dynamic performance comparasion at 311 V - 411 V step input voltage (a) Analog ACMC (b) Digital ACMC

Table 2. Steady state current regulation of Analog ACMC based QBC

Analog ACMC based QBC		
Input voltage	**Steady state load current deviation (i_o) in mA**	$\frac{\Delta io}{Rated\ load\ current} \times 100\%$
311V	±0.45	±2.25
211V	-0.5	-2.5 (Peak)
411V	+0.58	+2.9 (Peak)

Table 3 Steady state current regulation of Digital ACMC incorporated QBC

Digital ACMC based QBC		
Input voltage	**Steady state load current deviation (i_o) in mA**	$\frac{\Delta io}{Rated\ load\ current} \times 100\%$
311V	±0.1	±0.5
211V	+0.2	+1.0 (Peak)
411V	±0.8	±4.0

Table 4 Dynamic current regulation of Analog ACMC based QBC

Analog ACMC based QBC		
Step Input voltage	**Transient current deviation (mA)**	**Transient settling time (msec)**
311 V – 211 V	-0.58	2.0
311 V – 411 V	+0.1	1.0

Table 5 Dynamic current regulation (DCR) of Digital ACMC based QBC

Digital ACMC based QBC		
Step Input voltage	**Transient current deviation (mA)**	**Transient settling time (msec)**
311 V - 211 V	-0.4	1.0
311 V - 411 V	+0.02	0.5

Fig. 13 depicts the efficiency Vs LED string current curves at different QBC input side dc voltages of 311 V, 271 V, 231 V and 191 V. The LED string current variation is figured out from 10 mA to 80 mA. For this current variation, much more efficiency downfall is pronounced at 311 V as

compared to 191 V. It is seen that, 54.7776% and 82.3344% are the lowest and highest efficiencies occurring at 311V, 10 mA and 191 V, 40 mA respectively. At rated LED string current of 20 mA, the efficiency is close to 70%. The efficiency can be further aggrandized with the integration of synchronous rectification.

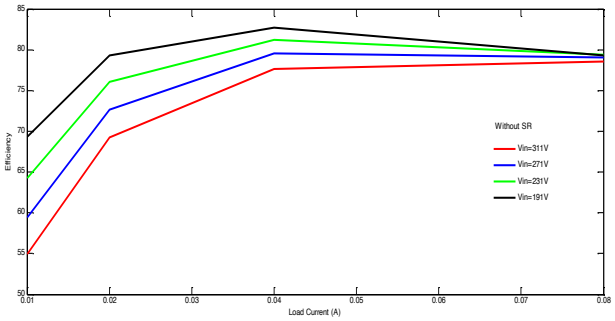


Fig. 13. Efficiency Vs. load curves at different input voltages

At rated load conditions of 20 mA and for 100 kHz - 900 kHz switching or operating frequency variation, the distribution of various converter losses are represented in Fig. 14. The dominant losses are the output capacitor losses followed by the reverse recovery losses. The least significant losses are the gate circuit losses.

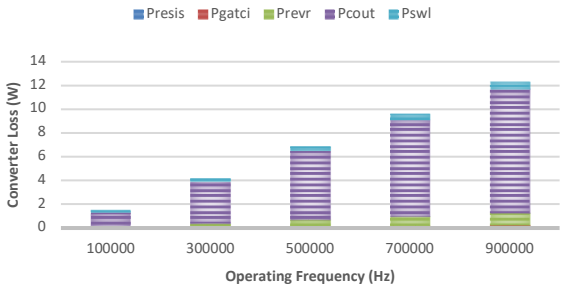


Fig. 14. Distribution of converter losses at rated load conditions

Fig. 15 shows the effect of operating frequency on the topology efficiency. The curves are shown for the 100 kHz - 900 kHz switching frequency variation at different load currents of 10 mA, 20 mA, 40 A and 80 mA. At rated load current of 20 mA, the efficiency alters by 57.51% under the considered operating frequency variation. The least and highest efficiency change occurrences are 27.0517% at 80 mA and 57.54% at 10 mA. This analysis is helpful in view of optimizing the switching frequency. As operating frequency increases, it gives a significant advantage of reduction in the converter size and thereby cost. However, the demerit is the diminished efficiency. Therefore, the operating frequency selection depends on the trade-off or compromise between the efficiency and cost. Fig. 16 shows the effect of duty cycle on the topology efficiency. The highest and lowest duty cycle variations are 0.986 and 0.659. The observed least and highest efficiencies are 23.3894% and 73.9864% at the duty cycles and load currents of 0.66, 10 mA and 0.986 and 80 mA respectively.

The discrete or digital ACMC based QBC has proven the superior performance in terms of the stability, converter dynamics and LED current regulation as compared to the analog ACMC based QBC. However, it is important to focus on the implementation cost of both the controllers. The real-time implementation of the digital ACMC based QBC requires PCB board, digital signal controller (DSPIC30F4011), passive resistors, passive capacitors, MOSFET gate driver (NCP5106ADR2G), potentiometer POT (P160KNP-0QC20A500K), current sensing resistor (WSLP27261L000FEA) and soldering components. All these digital control circuit components cost around $16.7. On the other hand, the implementation of the analog ACMC based QBC requires the essential components such as PCB board, passive resistors, passive capacitors, zener diodes (1N4749A), general purpose diodes (1N4148), potentiometer POT (P160KNP-0QC20A500K), precision shunt voltage reference (LM4041BIM3-1.2+T), op-amps (MCP6142T-I/MS), PWM controller (NCP1034DR2G), MOSFET gate driver (NCP5106ADR2G), current sensing resistor (WSLP27261L000FEA) and other soldering components. The overall cost estimation of these components is around $20.7. Therefore, the implementation cost of the digital ACMC based QBC gets reduced by nearly 19.4% as compared to the analog ACMC based QBC. The overall implementation cost of the discrete ACMC based QBC is almost in propinquity to that of the analog ACMC based QBC. The above cost estimation and comparison are fulfilled at the purchase of one unit quantity. If considered for more number of units in case of bulk manufacturing then the cost decreases further. Also, the discrete ACMC based QBC is superfluous with phenomenal advantages such as occupying less space, noise immunity, free from parameter drift, considering nonlinearities, realizing complex algorithms and more reliable.

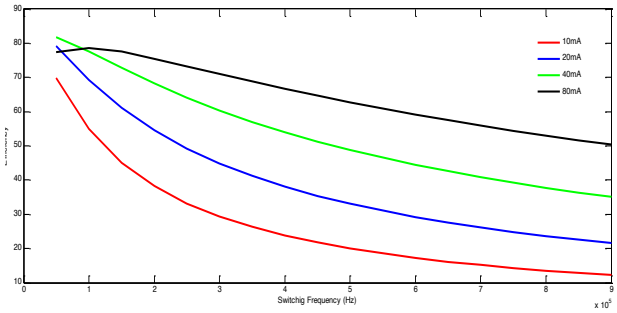


Fig. 15. Variation of efficiency with respect to the switching frequency at different load currents

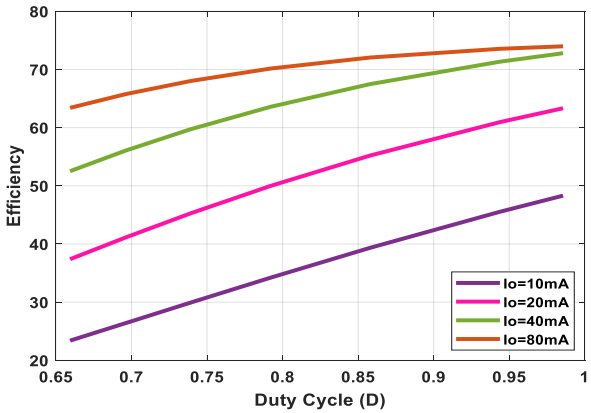


Fig. 16. Variation of efficiency with respect to the duty cycle at different load currents

5. Conclusions

This paper emphasizes the features and performance of QBC with ACMC and Digital ACMC for LED lighting

applications. The PSIM simulation results are interpreted for the steady state as well as line regulations with the aid of different case studies. The digital ACMC based QBC has exhibited phenomenal performance with a steady current regulation ±0.5% as opposed to ±2.25% in case of the analog ACMC based QBC. On the other hand, the dynamic settling time of 1 msec is achieved in case of the digital ACMC based QBC as opposed to the analog ACMC based QBC with 2 msec. Importantly the transient current dip is only 0.4 mA in the digital ACMC based QBC as compared to the analog ACMC based QBC with 0.58 mA. Moreover, the implementation cost of the digital ACMC based QBC gets reduced by nearly 19.4% as compared to the analog ACMC based QBC. The adoption of the digital ACMC based QBC can be the righteous option for LED lighting applications. This work can be further preferred for wide power levels of the QBC.

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