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Fault-tolerant and Area-efficient EXOR Circuit Design using QCA Nanotechnology

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Abstract

Quantum-dot cellular automata (QCA) nanotechnology offers efficient design of digital circuits. High-speed, low-energy consumption, low-area requirement are the significant features of QCA nanotechnology. An exclusive-OR (EXOR) gate has been applied to design various digital applications. Hence, an efficient EXOR gate design needs to be implemented. This research work proposes a translation-based three input EXOR gate in QCA nanotechnology. The proposed EXOR gate is extensively explored for fault analysis. The power dissipation analysis is also given for the proposed EXOR gate. The proposed EXOR gate has only 10 cells and two clock latencies. For the performance evaluation of the proposed EXOR gate, a comparative analysis is provided for different parameters. The proposed EXOR gate outperforms in comparison to the existing EXOR gates in QCA nanotechnology. It improves the cell area by 25% and the layout cost by 23.08% in comparison with the best-reported three input EXOR gate in the literature. The efficacy of the proposed three input EXOR gate for the digital circuit implementation is noted by designing a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit binary to gray (B2G) code converter.

Keywords: Quantum-dot cellular automata, exclusive-OR, power maps, fault analysis, translation method.

1. Introduction

The revolution in the field of electronics is much needed to overcome the shortcomings of transistor technology. The progress made in QCA nanotechnology is the foundation for future electronics systems. The logic fabrication, based on transistor technology, is quite difficult in ultra-nanometer range of devices due to many effects. Therefore, exploration of the transistor-free method is much more important in the current situation. QCA nanotechnology is a suitable choice in the ultra-nanometer range of circuit design because of the generation of digital logic without any transistor structure [1-3]. QCA nanotechnology avoids all the shortcomings of complementary metal oxide semiconductor (CMOS) technology in the ultra-nanometer range. The scaling of the size of devices in the ultra-nanometer range is the biggest drawback for CMOS technology [4-6]. But it is indeed a required operation to reduce the size of portable systems. So, QCA nanotechnology not only reduces the size of the logic circuits but also it gives high-speed and energy-efficient operations.

The EXOR gate is a fundamental element for various operations in digital system design. An effective EXOR gate is the backbone of high-performance electronics systems. Therefore, this paper proposes a novel idea of a QCA-based three input EXOR gate using a translation method, where the output QCA cell is shifted by a half distance to produce the actual logic function. The comprehensive analysis of the proposed EXOR gate and comparison with the existing works are delivered in the paper. The proposed EXOR gate is further used for the design of a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit B2G code converter to judge its implementation for other applications.

The remaining part of this paper is ordered as follows: the fundamentals of QCA nanotechnology are explored in Section 2. Section 3 proposes a novel structure for the EXOR gate with fault analysis and power dissipation. The design of a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit B2G code converter are discussed in Section 4. The comparative analysis is presented in Section 5. At last, the paper is concluded in section 6.

2. Fundamentals of QCA nanotechnology

QCA nanotechnology comprises a cell, which is used for logic implementations. A QCA cell is a basic structure, containing four quantum dots. The locations of quantum dots are allocated at the corners of a square shape. The electrons are distributed in these quantum dots in a cell. Two electrons are possible in four quantum dots and two quantum dots are free for the movement of electrons. Based on the location of the electrons, a binary value can be generated [7-9]. Binary values 0 and 1 using a QCA cell are noted in figure 1.

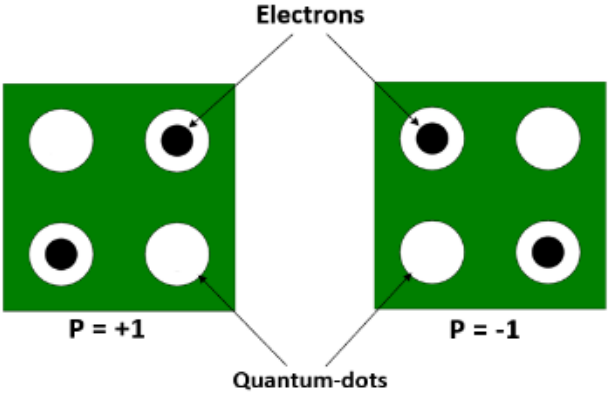

Fig. 1. Binary values in a QCA cell

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QCA nanotechnology doesn't require a power supply. Hence, energy dissipation is negligible in QCA nanotechnology. However, logic formation needs some energy to execute the operation. The need for energy is fulfilled by a clocking scheme in QCA nanotechnology. Therefore, the clocking scheme in QCA nanotechnology is the backbone for logic formation. The clocking scheme consists of four zones and four phases. All the successive phases in QCA nanotechnology are distributed 90° with each other. The four phases are switch, hold, release, and relax [10-12]. The inter-dot barrier potential for all the phases is depicted in figure 2.

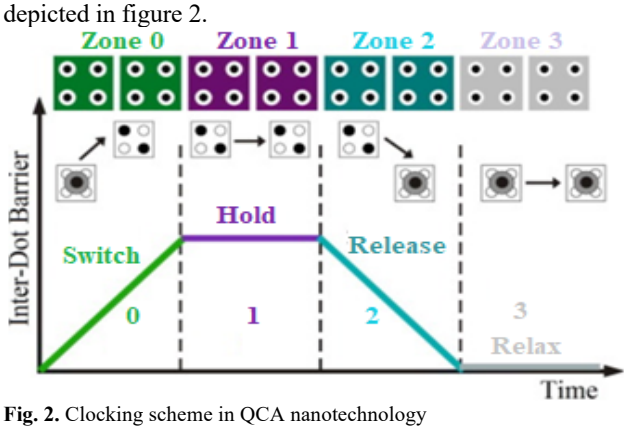
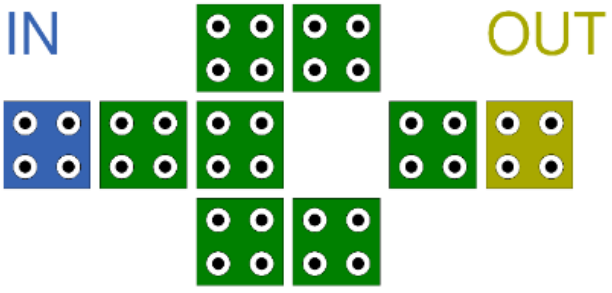


Fig. 2. Clocking scheme in QCA nanotechnology

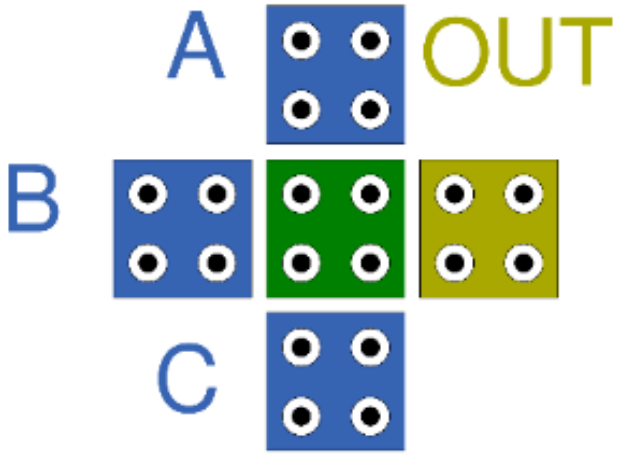
The wiring requirement is also present in QCA nanotechnology. The wiring in QCA nanotechnology is nothing; it is the connection of QCA cells in a horizontal or vertical direction. A combination of the number of cells in the horizontal or vertical direction forms a wiring system. Different phases may also be applied to form a wiring system in QCA nanotechnology [13-15]. A wiring system with different phases is shown in figure 3.

Fig. 3. Wiring system in QCA nanotechnology

Digital system design involves the fundamental logic gates. The inverter, AND, and OR are the primary logic gates, which are needed for Boolean function generation. Hence, these primary logic gates are also implemented in QCA nanotechnology. There is a concept of majority voter in QCA technology for the design of AND and OR gates. There are different ways to layout the inverter and majority voter circuits in QCA nanotechnology [16-19]. The primarily used inverter and majority voter circuits are presented in figure 4.



(a)



(b)

Fig. 4. Primary gates in QCA nanotechnology (a) inverter (b) majority voter

3. Proposed three input EXOR gate

The EXOR is a key module for higher-order systems such as comparators, ALUs, adders, subtractors, code converters, parity generations & checkers, etc. So, designing the EXOR gate is very important to optimize the performance metrics of the circuits. The improved metrics enhance the overall evaluation of the circuits in the nanometer range. The EXOR gate produces a binary value of 1 only if an odd number of 1's is available at the inputs. If the number of 1's is even at the inputs of a gate, then it is treated as an EXNOR gate, which is the complement form of an EXOR gate. Hence, EXOR and EXNOR gates can be easily designed by using an inverter circuit. The truth table of the proposed three input EXOR gate is presented in table 1.

Table 1. Input combinations for EXOR gate

Input combinations	Output
000	0
001	1
010	1
011	0
100	1
101	0
110	0
111	1

Table 1 is used for the formation of Boolean function. The output logic functions of three input EXOR and EXNOR gates are given in equations 1 and 2, respectively.

$$Y(EXOR) = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \quad (1)$$

$$Y(EXNOR) = \overline{Y(EXOR)} \quad (2)$$

A translation method can be utilized in QCA nanotechnology, where a few QCA cells are shifted by a distance. The traditional QCA circuits can't allow any distance shifting of QCA cells in logic circuits, which may cause additional cell and clock requirements in a QCA circuit. The translation method allows the QCA cells to shift by a distance, but the distance must be less than 18 nm. Otherwise, it will be full-distance shifting, causing a traditional implementation. The cell translation effect is able

to generate proper logic functionality in QCA circuits with fewer QCA cells and clocks.

A translation method-based EXOR gate is proposed in this paper by counting a half-distance translation. The half-distance translation produces the desired output without any complexity. A QCA cell has a dimension of $18\,nm \times 18\,nm$. So, the half-cell width is 9 nm. A three input EXOR gate is proposed, which can be easily extended to two inputs, four inputs, five inputs, and so on. Figure 5 shows a three input (A, B, and C) EXOR gate using QCA nanotechnology with a schematic and output response. The QCA layout and simulation response are extracted through the QCA Designer-E tool for the default values of the bistable simulation engine.

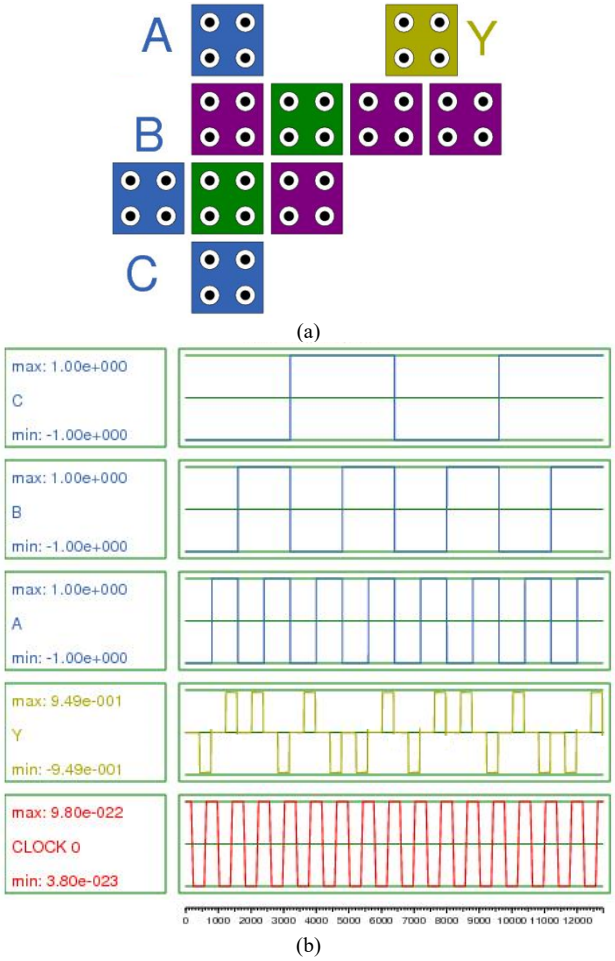


Fig. 5. Proposed three input EXOR gate in QCA nanotechnology (a) schematic (b) output response

The cell count of the proposed three input EXOR gate is 10 and the latency is 0.5. The cell area of the proposed EXOR gate is 3240 nm^2 and the layout area is 6480 nm^2. The output response in figure 5 witnessed the accurate behaviour of the proposed EXOR gate. There is no need for any crossover or multi-layer configuration for the proposed three input EXOR gate.

The defects in the QCA-based circuits are also possible due to a single cell addition and a cell missing. These defects may occur at the time of the fabrication or logic construction of circuits. The faults may affect the overall functionality of the circuits. Hence, fault analysis is essential to estimate the possible fault values. These faults represent the prediction against cell addition and cell omission defects. There may be many reasons for the faults, like cell negligence, error, implementation layer, circuit complexity, cell distribution, etc. The faults are estimated by considering all possibilities in a QCA layout. The logic function may fail if there are tightly connected cells in a structure, like in the cell interaction method, which uses charge flow in a defined way to minimize the cell count and latencies. A cell grid structure with numbering is utilized for the calculation of faults for the proposed EXOR gate. The cell grid structure is given in figure 6 to easily identify the defects due to cell addition and cell missing.

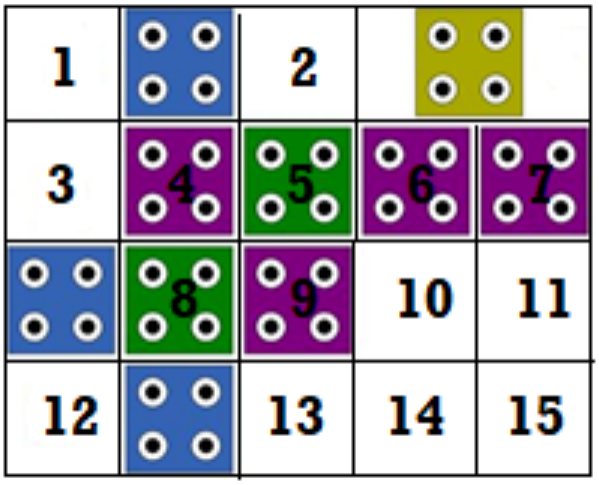


Fig. 6. Cell grid structure for the proposed EXOR gate

The cell missing defects are possible due to cell numbers 4, 5, 6, 7, 8, and 9. The cell addition defects are produced because of the extra insertion of QCA cell in 1, 2, 3, 10, 11, 12, 13, 14, and 15 positions. In the case of a single cell addition defect, an extra cell is inserted in the grid structure and the response is checked for logic failure. Similarly, a QCA cell is missing in cell positions 4, 5, 6, 7, 8, and 9 to judge the impact of the cell missing defect. Input and output cells are fixed and assumes no deviation is there. The fault values are compared with the exact output of the proposed EXOR gate, i.e., 01101001, for each possible combination. Table 2 lists the possible fault values.

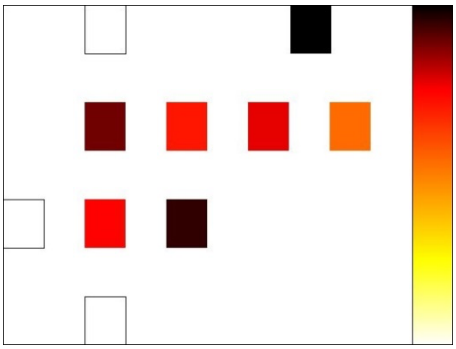
Table 2. A single cell addition and a cell missing defects

Defect	Cell number	Output (Exact = 01101001)	Fault count
Addition	1	01101001	0
Addition	2	11001100	4
Addition	3	01101001	0
Missing	4	00110011	4
Missing	5	00010111	6
Missing	6	11101000	2
Missing	7	11101000	2
Missing	8	00110011	4
Missing	9	00001111	4
Addition	10	01101001	0
Addition	11	01101001	0
Addition	12	01101001	0
Addition	13	10101010	4
Addition	14	01101001	0
Addition	15	01101001	0

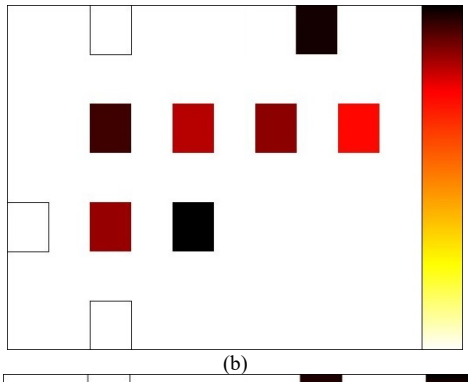
It is observed from table 2 that there are a total of 30 faults out of a total of 120 combinations. Hence, the proposed EXOR gate is $100 - 25 = 75\%$ fault tolerant. It is also seen from table 2 that cell missing is dominant in

comparison with cell addition. A single cell missing contributes a total of 22 faults, while a single cell addition contributes only 8 faults. The proposed EXOR is designed using a cell translation method with tightly connected cells. Therefore, any cell missing in this structure causes logic failure.

The estimation of energy dissipation is also important in QCA circuits. The energy is transferred from input cells to output cells and a small amount of energy is dissipated into the environment. The energy dissipation analysis for the proposed EXOR gate is done with the QCA Pro tool for different kink energies. It also gives the power maps. The power map shows the cell-by-cell power dissipation. The dark cells depict more power dissipation. The power maps for the proposed EXOR gate at different kink energies are represented in figure 7.



(a)



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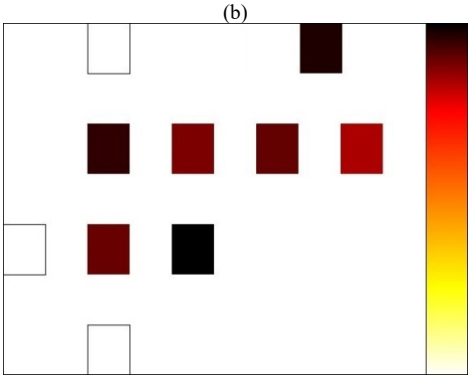


(c)

Fig. 7. Power dissipation map for kink energy (a) $E_k = 0.5$ (b) $E_k = 1$ (c) $E_k = 1.5$

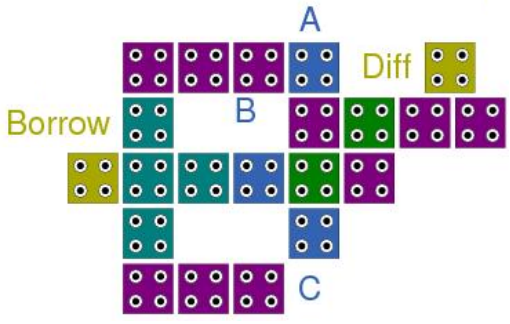
The average values of leakage and switching energy dissipations for the proposed EXOR gate are provided in table 3. The total energy dissipation is the sum of leakage and switching energy dissipation values at the respective kink energy levels.

Table 3. The values of energy dissipation for the proposed EXOR gate

Average leakage (meV)			Average switching (meV)			Total (meV)		
$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$	$0.5E_k$	$1E_k$	$1.5E_k$
3.46	8.62	14.01	5.62	4.41	3.54	9.08	13.03	17.55

4. Circuit designs using the proposed EXOR gate

The proposed three input EXOR gate is applied for the formation of logic circuits such as a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit B2G code converter. This section discusses the QCA designs of a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit B2G code converter. These circuit designs reflect the efficacy of the proposed EXOR gate for multi-bit operations and the ease of the gate. A full subtractor is implemented by a proposed EXOR gate and a majority voter. The QCA schematic and output response of the full subtractor are presented in figure 8.



(a)

(b)

Fig. 8. 1-bit full subtractor using the proposed EXOR gate (a) schematic (b) response

The proposed full subtractor using the proposed EXOR gate consists of a single layer and 21 cells only. The developed full subtractor contained the idea of one three input majority voter for borrow generation and one three

input EXOR gate. The output response in figure 8 shows the accurate behaviour of the developed full subtractor.

The parity checker is utilized in the communication system to detect the parity bit at the destination. The parity checker may detect the even or odd parity bits. A 4-bit parity checker checks the nature of the parity bit. An even parity checker is proposed with the help of the proposed three input EXOR gate. For the generation of 4-bit inputs, two proposed three input EXOR gates are needed. The schematic and output response of the 4-bit parity checker are provided in figure 9 in QCA nanotechnology.

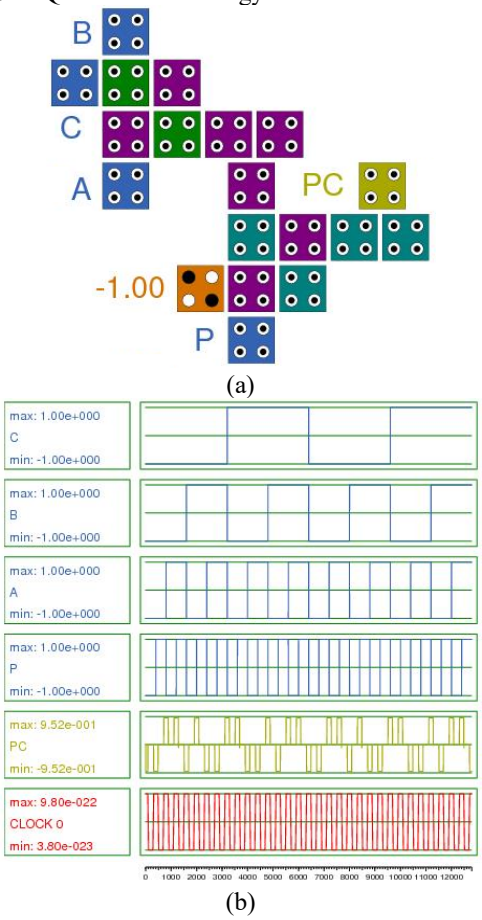


Fig. 9. 4-bit parity checker using the proposed EXOR gate (a) schematic (b) response

There are only 19 cells required in the proposed 4-bit parity checker circuit using the proposed three input EXOR gate. The output response, as shown in figure 9, confirmed the accurate output of the proposed 4-bit even parity checker using the proposed EXOR gate.

The gray code is a unit distance code and is very useful in many applications and k-map designs. Therefore, a 4-bit B2G code converter is also designed using the proposed EXOR gate. Fundamentally, B2G requires an EXOR operation. The QCA-based schematic and output response for the 4-bit B2G code converter are shown in figure 10. The simplest way is used for the formation of a B2G code converter, where the proposed three input EXOR gate is applied as two inputs and consecutive bits are the EXOR operation. The proposed B2G code converter uses only 32 cells and 0.5 latency on a single layer.

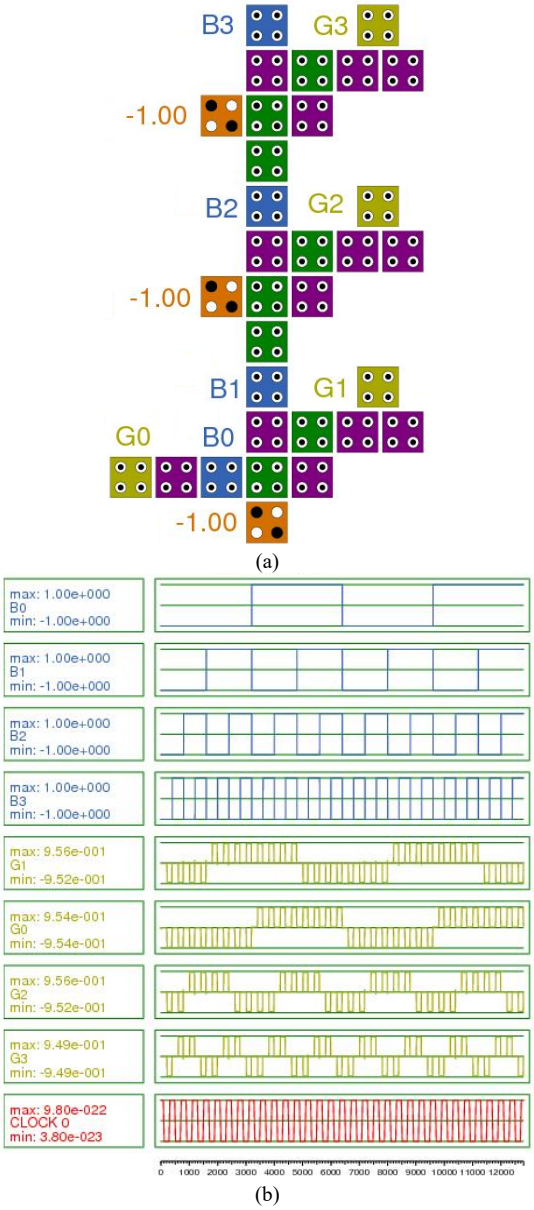


Fig. 10. 4-bit B2G code converter using the proposed EXOR gate (a) schematic (b) response

5. Comparison analysis

This section is devoted to the comparative analysis of the proposed three input EXOR gate and the other circuits designed using the proposed EXOR gate with the existing ones on several parameters. The parameters, like cell count, total area, cell area, delay, and cost are defined for performance comparison. The defined parameters are the key assessment factors in QCA nanotechnology. Table 4 details the comparative values for the proposed three input EXOR gate, a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit B2G code converter.

Table 4. Proposed designs comparison with the existing ones

Design	Cell Count	Total Area (μm^2)	Cell Area (μm^2)	Delay	Cost
Three input EXOR gate					
[20]	17	0.016	0.006	0.50	0.136
[21]	14	0.006	0.005	0.50	0.042

[22]	11	0.008	0.004	0.50	0.044
[23]	14	0.012	0.005	0.50	0.084
[24]	11	0.007	0.004	0.50	0.039
[25]	14	0.010	0.005	0.50	0.070
[26]	12	0.010	0.004	0.50	0.060
Proposed	10	0.006	0.003	0.50	0.030
1-bit full subtractor					
[27]	29	0.019	0.009	0.75	0.413
[28]	52	0.032	0.017	0.50	0.832
[29]	63	0.043	0.020	0.75	2.032
[30]	136	0.136	0.044	1.75	32.368
[31]	83	0.078	0.027	0.75	4.856
[32]	37	0.032	0.012	0.75	0.888
[33]	58	0.039	0.019	1.00	2.262
Proposed	21	0.013	0.007	0.75	0.205
4-bit parity checker					
[34]	85	0.073	0.028	1.25	7.756
[35]	87	0.072	0.028	1.75	10.962
[36]	85	0.078	0.028	1.25	8.288
[37]	40	0.035	0.013	0.50	0.700
[38]	92	0.087	0.030	1.75	14.007
[39]	118	0.170	0.038	1.25	25.075
Proposed	19	0.017	0.006	0.75	0.242
4-bit B2G code converter					
[40]	107	0.140	0.035	0.75	11.235
[41]	99	0.067	0.032	0.75	4.975
[42]	92	0.100	0.030	0.75	6.900
[43]	39	0.050	0.013	0.25	0.488
[44]	48	0.060	0.016	0.50	1.440
[45]	39	0.031	0.013	0.50	0.605
Proposed	32	0.027	0.010	0.50	0.432

A total number of cells utilized for circuit structures is treated as a cell count. The occupied layout area is the total area of the circuits. The cell area depends on the cell count and the dimension of a cell. The delay is counted in term of clock phases. Two key metrics of the QCA circuits are cell count and clock delay, and these two metrics affect the overall performance parameters and efficiency of the logic circuits. The layout cost is the product of the cell count, total area, and delay of the circuits. For a cost-effective design, the calculated cost must be minimized, which ultimately depends on the proper execution of the logic structures.

In table 4, only the existing three input EXOR gates are compared for fair comparison. It is observed from table 4 that the proposed EXOR gate is not only optimized in term of cell count but also it is cost effective. Very limited three input EXOR gates are available in the literature. All the performance parameters are improved in the case of the proposed EXOR gate, which ultimately improves the metrics for other circuits that are also designed using the proposed EXOR gate. A minimum of 11 QCA cells are needed for the three input EXOR gate, as available in the literature, while the proposed EXOR consists of only 10 cells. A lower count improves the cell area. The total area is also improved in the proposed EXOR gate because of the logic structure in comparison to the existing ones. The delays of all EXOR gates are the same, while their cell count and total area contribute to the layout cost. Figure 11 presents the graphical representation of cell count and layout cost for the proposed three input EXOR gate.

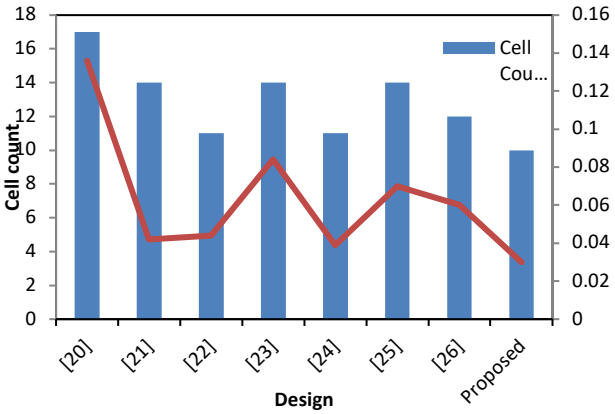


Fig. 11. A cell count and the layout cost of the various EXOR designs

6. Conclusion

QCA nanotechnology has the full potential to develop digital systems for future technologies. QCA nanotechnology not only overcomes the short-channel issues of CMOS technology but also improves speed, energy dissipation, and area overhead. An EXOR gate is the backbone of many digital applications. Therefore, a three input EXOR gate is proposed in the paper using QCA nanotechnology. The fault-analysis and power dissipation maps are checked for the proposed EXOR gate. There is a need of 10 QCA cells and 0.50 of latency in the proposed EXOR gate. The proposed EXOR gate is further applied to design a 1-bit full subtractor, a 4-bit parity checker, and a 4-bit B2G code converter in QCA nanotechnology to check its effectiveness. A comparative analysis is also presented of the proposed designs with the existing ones to show the importance of the

proposed circuits. All the performance metrics are improved in the proposed designs as compared to the existing ones. The proposed 1-bit full subtractor, 4-bit parity checker, and 4-bit B2G code converter are 50.36%, 65.43%, and 11.48%, respectively, cost-effective as compared to the best-reported similar work in the literature. So, the proposed EXOR gate is very useful for the implementation of future digital systems.

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