Journal of Engineering Science and Technology Review 18 (2) (2025) 49- 57

Research Article

JOURNAL OF
Engineering Science and Technology Review

www.jestr.org

Performance Estimation of Dual-Halo Dual-Material Silicon-On-Insulator with High-K Dielectrics for Low Power Applications

Pawan[1,*], Nitin Sachdeva[2], Rohtash Dhiman[3], Shailendra Narayan Singh[4], Swati Sharma[5], Rachna Jain[6] and Vinod Kumar Panchal[7]

[1]Department of CSE(AI&ML), Meerut Institute of Engineering & Technology, Meerut, Uttar Pradesh, India
[2]Department of Electronics Engineering, J.C. Bose University of Science and Technology, Faridabad, Haryana, India
[3]Department of Electrical Engineering, DCRUST Murthal, Haryana, India
[4]Department of CSE, Meerut Institute of Engineering and Technology, Meerut, Uttar Pradesh, India
[5,7]Department of CSIT, Meerut Institute of Engineering and Technology, Meerut, Uttar Pradesh, India.
[6]Department of IT, Bhagwan Parshuram Institute of Technology, Rohini, Delhi, India

Received 21 November 2024; Accepted 21 March 2025

Abstract

A novel silicon-on-insulator (SOI) MOSFET is proposed and investigated in this paper. The existing structure is modified by adding uniform dual halo implants in the drain and source side. Ultra-thin SOI involves using an extremely thin silicon layer on an insulating substrate. This approach offers improved electrostatic control, reduced short-channel effects, and enhanced transistor performance due to better gate control over the thin channel region. The incorporation of dual material and high K material leads to enhancements in the sub-threshold leakage current, sub-threshold slope, DIBL, ON/OFF ratio and other short channel effects as compared to standard SOI-MOSFET. The combination of dual halo and dual material engineering aims to take advantage of the benefits each technique offers. Dual halo engineering helps to control the behavior of the transistor near the source and drain regions, reducing leakage and improving control. Dual material engineering allows for optimizing the channel region for enhanced performance. Dual Halo Dual Material Silicon-On-Insulator (DHDM) SOI MOSFETs aims to provide improved performance, reduced leakage, enhanced electrostatic control, and efficient operation due to their unique combination of design strategies. The proposed device is designed following the International Technology Roadmap for Semiconductors (ITRS) rules and can be further proposed for next-generation semiconductor Nano-scale devices.

Keywords: Silicon-On-Insulator **(**SOI), Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Fully Depleted Silicon-On-Insulator (FDSOI), Technology Computer-Aided Design (TCAD)

1. Introduction

The semiconductor industry is a critical sector of the global economy that plays a fundamental role in the design, manufacturing, and distribution of semiconductor devices. These devices, which include integrated circuits (ICs) or microchips, serve as the building blocks for electronic devices across various industries, from consumer electronics to industrial automation and healthcare. Over the last 25 years, silicon technology has emerged as the dominant technology in the microelectronics field because of the need for high integration density and high-performance digital circuits. In traditional bulk silicon technology, transistors are built directly on a silicon substrate [1]. Scaling refers to the continuous reduction in the size of transistors and other components in integrated circuits. Scaling has been a fundamental driving force behind the advancements in semiconductor technology, leading to increased transistor density, improved performance, and reduced power consumption. The process node is a measure of the smallest feature size on a microchip, often measured in nanometres (nm) [2]. Smaller transistors consume less power while switching, leading to improved energy efficiency. This is crucial for portable devices like smartphones and laptops, where battery life is a significant concern. However, as transistors continue to shrink, several scaling issues arise that can negatively impact device performance and pose challenges for further miniaturization [3].

As transistor channel length shrinks, short-channel effects such as Drain-Induced Barrier Lowering (DIBL) and Sub-threshold Leakage become more prominent [4,5]. These effects can cause undesirable changes in device characteristics and increase leakage current. To mitigate short-channel effects, device architectures such as Fin Field Effect Transistor (FinFETs) and nanowire transistors have been introduced, offering better control over channel electrostatics and reduced leakage. As the oxide layer thickness is scaled down, gate leakage current increases, leading to higher power consumption. High-K dielectrics (materials with high dielectric constant) and metal gate electrodes have been adopted to replace traditional silicon dioxide as gate insulators, effectively reducing gate leakage [6]. Shrinking dimensions amplify the impact of process variations, leading to device performance variations across a chip. Statistical design techniques, improved process control, and design optimizations can help mitigate these variations and ensure reliable device operation [7]. To overcome these scaling issues and continue advancing semiconductor technology, researchers and industry professionals are actively investigating new materials, device architectures, and fabrication techniques.

The continuous scaling of MOSFET dimensions deteriorates the performance of the device and enables

*E-mail address: panchalpawan16987@gmail.com
ISSN: 1791-2377
doi:10.25103/jestr.182.07

different innovations such as Silicon-on-Insulator (SOI) to be developed by emerging technology. Two types of SOIs are available: PDSOI (Partially depleted SOI) and FDSOI (Fully depleted SOI). Due to its stronger sub-threshold slope along with small parasitic capacitance, FDSOI MOSFET is preferable. In SOI technology, a thin layer of silicon is separated from the bulk substrate by an insulating layer which prevents the flow of electrical current between the active silicon layer and the bulk substrate [8]. SOI MOSFETs have reduced leakage current and high speed due to very low capacitance and lower power dissipation as compared to traditional MOSFETs. The thickness of buried oxide can be varied to get a high-performance device. SILVACO TCAD tool is used to evaluate the Dual material SOI MOSFET behavior [9]. To decrease the leakage current of the device which is the necessary parameter in MOSFETs presently, the channel is doped with halo implants. The threshold voltage of the device can be adjusted by increasing or decreasing the doping concentration of the channel [10,11]. The leakage current of the MOSFET is a crucial metric for determining the capability of the device. This proposed device is essential for developing higher-speed, lower-power and more scalable devices, making it valuable for 6G communication systems. It is well-suited for applications requiring low power consumption, such as mobile devices and wireless communication system. The high speed and low power of SOI devices are vital for the processing of large amounts of data in 6G networks. SOI wafers are also used in silicon photonics to fabricate optical waveguides and other passive optical devices, which are crucial for high-speed data transmission in 6G infrastructure.

Contributions of this paper

- The research intends to explore this novel structure: DHDM-SOI Dual Halo Dual Material MOSFET with improved subthreshold leakage current, drain current, ON/OFF current ratio, and subthreshold slope.
- The device is designed and simulated using SILVACO ATLAS TCAD tool.
- The halo doping is performed on both sides of the channel in the Dual Halo Dual Material SOI device so that the best leakage current value can be obtained for low power applications.
- The influence of various MOS parameters i.e., silicon film thickness, work-function, applied drain voltages and effect of single & dual material gate on the leakage current has been studied.

2. Dual Material SOI MOSFET

The concept of Dual Material SOI MOSFETs aims to exploit the unique properties of different materials to enhance the performance of the transistor. By using two materials with distinct characteristics, such as different band gaps or carrier mobility, it becomes possible to optimize specific aspects of the device's operation. The use of Dual Material SOI in MOSFETs can provide advantages such as improved speed, reduced power consumption, and better control over device characteristics [12]. However, it also presents challenges in terms of material integration, manufacturing processes, and device reliability. Research on Dual Material SOI MOSFETs continues to explore the various material combinations, fabrication techniques, and device architectures to optimize performance and overcome challenges. It is an active area of research in semiconductor device technology with the potential to enable advanced and high-performance integrated circuits.

Due to the increased electric field on the drain side of the MOSFETs, various short channel effects occur which further reduce the device performance of the device. Gate material engineering is used to resolve these short channel effects and to decrease the strong electric field on the drain side [13]. To improve the electric field at the source region, the Dual Material device is proposed here to increase the efficiency of channel carriers. In the DMG MOSFET, the metal work function of Gate1 (M_1) is higher than that of Gate2 (M_2) and the threshold voltage corresponding to M_1 (Vt_1) is also higher than that corresponding to M_2 (Vt_2). It has the implied benefit of increasing gate transport efficiency by changing the electric field profile across the channel. Due to the distinct work functions of the two gates, the surface potential profile which is a step function validates a decrease in the short-channel effects and the screening of the channel region under the M_1 from the variations of the drain potential [14].

2.1 Dual Material Gate Structure

The structure of fully depleted Dual-Material SOI MOSFET with two metal gates M_1 and M_2 of lengths L_1 and L_2 respectively is shown below in Figure 1.

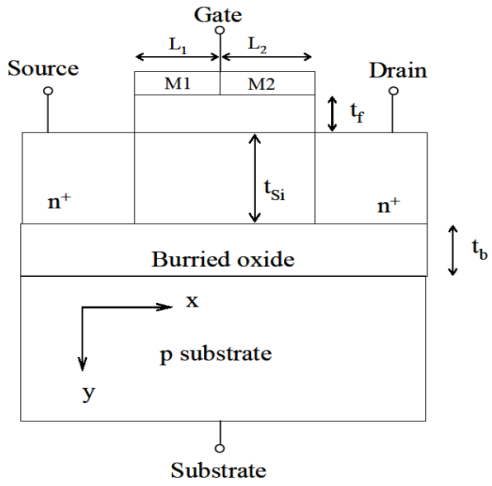

Fig. 1. Structure of Dual material SOI MOSFET

The source/drain regions of the device are doped uniformly at $9x10^{18}cm^{-3}$ and the channel is doped at $1x10^{15}cm^{-3}$. The buried oxide thickness, silicon channel thickness and front gate oxide thickness are 41nm, 9nm and 0.5nm respectively. The Source/Drain extension and channel length L_C (L_1+L_2) are considered 10nm and 15nm respectively. The work function of used materials M_1 and M_2 are considered 4.6 and 4.1 respectively. Hafnium oxide (HfO2) is employed in this device because it has a more dielectric constant (K=16), which improves the electrostatic control of the gate across the channel and the I_{ON}/I_{OFF} ratio. The simulation of the device to analyze various parameters is carried out using different models. For the electron generation/recombination consideration, SRH and auger models are used to calibrate the theoretical values with the simulated values which are enabled in the simulator. Newton trap method is preferred for simulation which is useful when the system of equations is strongly coupled and has quadratic convergence, the Drift-Diffusion Transport Model and the non-equilibrium Green's Function (NEGF) have been employed for this analysis. The non-equilibrium Green's function (NEGF) formalism provides a sound conceptual basis for the development of quantitative models for quantum transport [15].

2.2 Mathematical Modeling

This section describes the mathematical model of the fully depleted Dual Material MOSFET. As the channel region is doped uniformly, it is also possible to ignore the effects of fixed charge carriers to model the potential distribution. Assuming the impurity density in the channel region to be uniform, and neglecting the effect of the fixed oxide charges on the electrostatics of the channel, the potential distribution in the silicon thin film before the onset of strong inversion can be written as:

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{Si}} \quad for\ 0\le x\le L\ ,0\le y\le t_{Si} \quad (1)$$

where t_{si} is the thickness of the silicon film, L is the channel length, N_A is the concentration of silicon doping and silicon permittivity is ε_{si} . The potential profile in the vertical direction, i.e., the y-dependence of $\phi(x,y)$, can be approximated by a simple parabolic function for fully depleted SOI MOSFETs. The parabola function can be expressed as

$$\phi(x,y)=\phi_s(x)+c_1(x)y+c_2(x)y^2 \quad (2)$$

where the surface potential is φ(x) and c_1(x) and c_2(x) are the constants that are a function of x only to measure the vertical direction potential i.e. y-direction [16]. The gate of the device is separated into two sections in the Dual Material Gate structure i.e. Metal1 (M_1) and Metal2 (M_2) and the potential under M_1 and M_2 can be written as

$$\phi_1(x,y)=\phi_{s1}(x)+c_{11}(x)y+c_{12}(x)y^2 \quad for\ 0\le x\le L_1\ ,0\le y\le t_{Si} \quad (3)$$

$$\phi_2(x,y)=\phi_{s2}(x)+c_{21}(x)y+c_{22}(x)y^2 \quad for\ L_1\le x\le L_1+L_2\ ,0\le y\le t_{Si} \quad (4)$$

For both Gate regions with boundary conditions, the potential profile is separately determined:

At the intersection of the two distinct metals, the continuous surface potential is

$$\phi_1(L_1,0)=\phi_2(L_1,0) \quad (5)$$

At the intersection of the two distinct metals, continuous electric flux is

$$\left.\frac{d\,\phi_1(x,y)}{dx}\right|_{x=L_1}=\left.\frac{d\,\phi_2(x,y)}{dx}\right|_{x=L_1} \quad (6)$$

The electric flux at the oxide intersection is constant for both Metal Gates.

$$\left.\frac{d\,\phi_1(x,y)}{dy}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{S1}(x)-V'_{GS1}}{t_{ox}} \quad \text{for Metal1} \quad (7)$$

$$\left.\frac{d\,\phi_2(x,y)}{dy}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{S2}(x)-V'_{GS2}}{t_{ox}} \quad \text{for Metal2} \quad (8)$$

Where t_{ox} is the gate oxide thickness, $V_{FB1,f}$ and $V_{FB2,f}$ are the flat band voltages of the front gate of M_1 and M_2 respectively.

$$V'_{GS1}=V_{GS}-V_{FB1,f} \text{ and } V'_{GS2}=V_{GS}-V_{FB2,f}$$

The potential distribution then changes linearly while the surface potential is fixed. The potential at the source side is given by:

$$\phi_1(0,0)=\phi_{s1}(0)=V_{bi} \quad (9)$$

The potential at the drain side is given by:

$$\phi_2(L_1+L_2,0)=\phi_{s2}(L_1+L_2)=V_{bi}+V_{DS} \quad (10)$$

Where the built-in is potential, $V_{bi}={E_g}/{2}+V_T ln\,{N_A}/{n_i}$, n_i is the intrinsic concentration, N_A is the concentration. Electric flux at the back gate–oxide and back channel interface is continuous for both the materials of the front gate. It is constant for both the metal gates at the intersection of buried oxide and the back channel.

$$\left.\frac{d\,\phi_1(x,y)}{dy}\right|_{y=t_{Si}}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{SUB}-\phi_B(x)}{t_b} \quad \text{for Metal1} \quad (11)$$

$$\left.\frac{d\,\phi_2(x,y)}{dy}\right|_{y=t_{Si}}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{SUB}-\phi_B(x)}{t_b} \quad \text{for Metal2} \quad (12)$$

Region under Metal1

The further relations of potential can be obtained from equations (3), (7) and (11) for the area under Metal 1:

$$\phi_{S1}(x)+c_{11}(x)t_{Si}+c_{12}(x)t_{Si}^2=\phi_B(x) \quad (13)$$

$$c_{11}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{S1}(x)-V'_{GS1}}{t_f}=C_f\left(\frac{\phi_{S1}(x)-V'_{GS1}}{\varepsilon_{Si}}\right)$$

where $C_f=\frac{\varepsilon_{ox}}{t_f}$ (14)

$$c_{11}(x)+2c_{12}(x)t_{Si}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{SUB}-\phi_B(x)}{t_b}=C_b\left(\frac{V'_{SUB}-\phi_B(x)}{t_b}\right)$$

where $C_b=\frac{\varepsilon_{ox}}{t_b}$ (15)

By solving the equations (12), (13) and (14), we get

$$c_{12}(x)=\frac{V'_{SUB}+V'_{GS1}\left(\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)-\phi_{S1}(x)\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}{\left(1+2\frac{C_{Si}}{C_b}\right)} \quad (16)$$

Where $C_{si}=\frac{\varepsilon_{si}}{t_{si}}$

By substituting the values of c_{11}(x) from equation (14) and c_{12}(x) from equation (16) to equation (3), the potential distribution is given as:

$$\frac{d^2\phi_{Si}(x)}{dx^2}-\alpha\phi_{S1}(x)=\beta_1 \quad (17)$$

Where $\alpha=\frac{2\left(1+\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right)}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}$

$$\beta_1=\frac{qN_A}{\varepsilon_{Si}}-2V'_{GS1}\left(\frac{\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}\right)-2V'_{SUB}\left(\frac{1}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}\right)$$

By obtaining the second-order non-homogenous differential equation (17), Potential distribution can be described as:

$$\phi_{S1}(x) = Aexp(\lambda_1 x) + Bexp(\lambda_2) - \frac{\beta_1}{\alpha} \quad (18)$$

$$A + B - \frac{\beta_1}{\alpha} = V_{bi} \quad (19)$$

Region under Metal2

Similarly, for the region under Metal2 relations obtained from equations (4), (8) and (12):

$$\phi_{S2}(x) + c_{21}(x)t_{Si} \ + c_{22}(x)t_{Si}^2 = \ \phi_B(x) \quad (20)$$

$$c_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi_{S2}(x) - V'_{GS2}}{t_f} \ = C_f \left(\frac{\phi_{S2}(x) - V'_{GS2}}{\varepsilon_{Si}} \right)$$

where $C_f = \frac{\varepsilon_{ox}}{t_f}$ (21)

$$c_{21}(x) + 2c_{22}(x)t_{Si} \ = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{SUB} - \phi_B(x)}{t_b} \ = \ C_b \left(\frac{V'_{SUB} - \phi_B(x)}{t_b} \right)$$

where $C_b = \frac{\varepsilon_{ox}}{t_b}$ (22)

By solving the equations (16), (17) and (18), we get

$$c_{22}(x) = \frac{V'_{SUB} + V'_{GS2}\left(\frac{C_f}{C_b} + \frac{C_f}{C_{Si}}\right) - \phi_{S2}(x)\left(1 + \frac{C_f}{C_b} + \frac{C_f}{C_{Si}}\right)}{t_{Si}^2\left(1 + 2\frac{C_{Si}}{C_b}\right)} \quad (23)$$

By substituting the values of c_{21}(x) from equation (21) and c_{22}(x) from equation (23) to equation (4), the potential distribution is given as:

$$\frac{d^2\phi_{S2}(x)}{dx^2} - \alpha\phi_{S2}(x) = \beta_2 \quad (24)$$

Where

$$\beta_2 = \frac{qN_A}{\varepsilon_{Si}} - 2V'_{GS2}\left(\frac{\frac{C_f}{C_b} + \frac{C_f}{C_{Si}}}{t_{Si}^2\left(1 + \frac{2C_{Si}}{C_b}\right)} \right) - 2V'_{SUB}\left(\frac{1}{t_{Si}^2\left(1 + \frac{2C_{Si}}{C_b}\right)} \right)$$

By solving the second-order non-homogenous differential equation (24), Potential Distribution can be described as:

$$\phi_{S2}(x) = Cexp(\lambda_1(x - L_1)) + Dexp(\lambda_2(x - L_1)) - \frac{\beta_1}{\alpha} \quad (25)$$

3. Results and Discussion

The analytical model of the dual material SOI MOSFET is estimated in the above section. The simulations are also performed in the ATLAS simulator with the same boundary conditions to validate the proposed analytical model with the simulated results. The device is initially developed and simulated in compliance with ITRS guidelines. The channel length (L_G=L_1+L_2) is 15 nm, the thickness of oxide (t_{ox}) is 0.5 nm and the thickness of silicon is 9 nm. Due to the decrease in oxide thickness of the gate, the gate leakage current flows through the thin layer of oxide along with other short-channel effects. Gate work-function engineering with two distinct work-functions is proposed to minimize the short channel effects. Also, the low k oxide layer is substituted with the high k oxide layer to reduce the tunneling effect. HfO_2, which is a material with high permittivity, is taken for gate oxide material.

HfO_2 has a dielectric constant in the range of 20-25, making it one of the most effective high-k materials for modern transistor technology. It provides a good balance between performance and scalability. The dielectric constant of Al_2O_3 is lower (around 8-10) than that of HfO_2. TiO_2 has a very high dielectric constant (around 40-50), but it suffers from poor thermal stability and interface issues. HfO_2 has a wide band gap of around 5.8-6.0 eV, which helps it withstand higher voltages without breaking down, making it ideal for high-performance transistors. This also helps reduce gate leakage currents, which is a significant concern in modern CMOS devices. ZrO_2 has a similar bandgap to HfO_2 (~5.7-6.0 eV), but leakage currents can become a challenge, especially at smaller nodes. HfO_2 forms a good interface with silicon, but there can be some issues with interface defects that could affect performance, especially at very small scales. These defects are less problematic when using HfO_2 as a gate dielectric in SOI technology compared to other materials like TiO_2. TiO_2 has poor interface quality, which limits its effectiveness in practical semiconductor applications, especially at small node sizes. HfO_2 has excellent thermal stability, which is important in advanced semiconductor manufacturing where high temperatures are involved in processing. HfO_2 remains one of the most popular choices for high-k dielectrics in SOI technology due to its balanced dielectric constant, thermal stability, and relatively low leakage. However, Al_2O_3 is an attractive alternative in situations where interface quality is paramount, even though its lower dielectric constant limits its performance in some applications. ZrO_2 and TiO_2 offer interesting properties (e.g., higher dielectric constants), but they come with trade-offs such as higher leakage, lower thermal stability, and poor interface quality.

Table 1. Process parameters for SOI Design

Parameter	Values		
	DM-SOI	**SHDM-SOI**	**DHDM-SOI**
Thickness of oxide (Top)	0.5 nm (HfO_2)	0.5 nm (HfO_2)	0.5 nm (HfO_2)
Silicon thickness (Channel)	9 nm	9 nm	9 nm
Buried thickness (Oxide)	41nm	41nm	41nm
Source/Drain Extension Length	10nm	10nm	10nm
Channel Length, L_{ch}	15nm	15nm	15nm
Main Gate Work-function, Φ	Φ_1(Mo)=4.6eV	Φ_1(Mo)=4.6eV	Φ_1(Mo)=4.6eV
Auxiliary Gate Work-function, Φ	Φ_2(Mn)=4.1eV	Φ_2(Mn)=4.1eV	Φ_2(Mn)=4.1eV
Channel doping	$1x10^{15}cm^{-3}$	$1x10^{15}cm^{-3}$	$1x10^{15}cm^{-3}$
S/D doping	$9x10^{18}cm^{-3}$	$9x10^{18}cm^{-3}$	$9x10^{18}cm^{-3}$
Halo doping	-	$6x10^{18}cm^{-3}$	$6x10^{18}cm^{-3}$ (On both sides of the channel)

The device specifications are shown in Table 1 shown above. To minimize the sub-threshold leakage current of the device, a dual work-function technique is used i.e. Φ_1(Mo)=4.6eV at the source end and Φ_2(Mn)=4.1eV at the drain side along with high k material. The simulated structure is shown in Figure 2 below following the simulations carried out in the simulator.

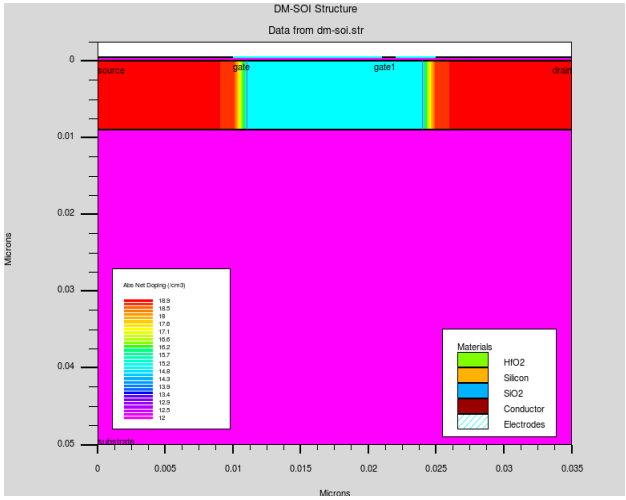

Fig. 2. Simulated Structure of DM-SOI MOSFET

By employing Molybdenum (Mo) for the M_1 gate and Manganese (Mn) for the M_2 gate as the Gate material, the dual metal is formed. The electric field is higher at the source end as compared to the drain end because of the high work function of the Metal M_1 at the source region. Visualizing this potential distribution in a graph might involve plotting the potential along the length of the channel from the source to the drain, with distinct regions showing varying potentials. However, the specifics of the graph, including slopes, gradients, and abrupt changes, heavily depend on the device's geometry, biasing conditions, doping concentrations, and other fabrication parameters. The surface potential of DM-SOI MOSFET has been analytically calculated and simulated at different drain voltages as shown in Figure 3.

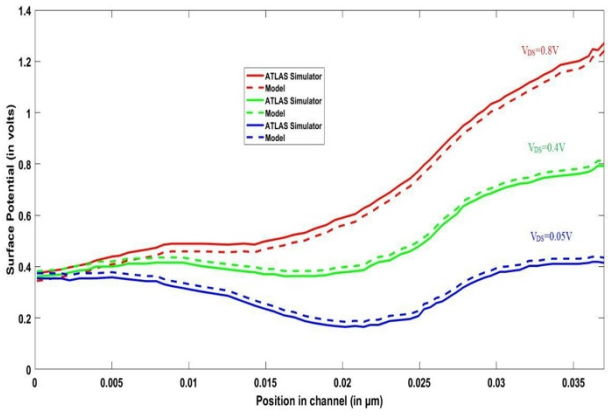

Fig. 3. Potential distributions Graph of DM-SOI MOSFET

The estimated and simulated surface potential values at various drain bias voltages are represented against the horizontal distance x for L=0.035μm in Figure 3. The simulation results validate the derived analytical model of the device. There is no substantial improvement in the potential under gate M_1 due to the presence of a dual-material gate, even though the drain bias is increased. Therefore, the drain voltage has a much lower effect on the drain current and decreases drain conductance. I_{DS}-V_{GS} (Drain-to-Source Current vs. Gate-to-Source Voltage) characteristics of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) change at different values of V_{DS} (Drain-to-Source Voltage). The I_{DS}-V_{GS} curves illustrate how the drain current varies concerning different gate-to-source voltages. While observing the I_{DS}-V_{GS} (Drain-to-Source Current vs. Gate-to-Source Voltage) characteristics on a logarithmic scale, particularly focusing on the leakage current (the small current that flows when the transistor is in the off-state), the behavior can be represented differently based on varying V_{DS} values. At low V_{DS} values, the logarithmic representation of the I_{DS}-V_{GS} curve in the off-state (when the transistor is supposed to be off) would display a nearly horizontal line. This line represents the extremely low leakage current that flows due to inherent factors like temperature and manufacturing imperfections. As V_{DS} increases, the logarithmic representation of the curve might show a slight upward slope in the off-state. This slope indicates a slightly higher leakage current than at lower V_{DS} values but still within the leakage current range for the transistor when it's supposed to be off. At higher V_{DS} values, the logarithmic plot might exhibit a steeper slope or an increase in the magnitude of the leakage current. This higher V_{DS} can cause an increase in the off-state leakage, which can become more pronounced in a logarithmic representation, showcasing a sharper incline on the graph. Monitoring leakage current is crucial, especially in applications requiring low-power consumption or where minimizing power dissipation in off-states is essential. Manufacturers aim to keep leakage currents as low as possible, particularly in technologies where power efficiency and standby power consumption are critical factors.

Dual Material Silicon-On-Insulator (SOI) refers to a technology where different materials are used to create the SOI substrate. This approach involves combining two different types of silicon materials within the SOI structure, typically to optimize certain properties of the transistors or integrated circuits fabricated on it. The traditional SOI structure consists of a thin layer of silicon (the active layer) on top of a thick layer of silicon dioxide (the buried oxide layer), which is on a bulk silicon substrate. The sub-threshold current alters linearly with the gate to the source bias. However, an exponential rise is visualized with an increase in the drain to source bias due to the barrier lowering induced by the drain. The increase in drain-source voltage boosts the lowest surface potential position which again exponentially increases the sub-threshold current [17]. So, for the shorter channel length devices, this exponential correlation becomes significant. For longer channel length devices, the leakage current is ignored but its influence cannot be ignored at smaller channel lengths. A higher leakage current gives increased energy consumption. It must also be taken into account at reduced lengths since it can give low power consumption. The I_{DS}-V_{GS} characteristics of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) represent the drain current (I_{DS}) as a function of the gate-source voltage (V_{GS}) at different drain-source voltages (V_{DS}). The I_{DS}-V_{GS} characteristics at different V_{DS} levels might show the shifting of these regions and the impact of drain voltage on the behavior of the transistor. The drain current of the DM-SOI has been measured at various drain voltages as shown in Figure 4. It has been observed that the drain current increases as the drain voltage of the MOSFET increases.

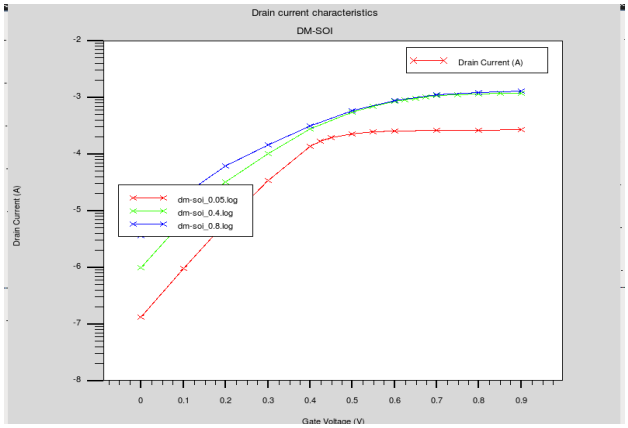

Fig. 4. I_{DS}-V_{GS} characteristics at different V_{DS}

The MOSFET is simulated with distinct work functions, i.e. Φ_1= 4.6eV and Φ_2= 4.1eV as shown in Figure 5 respectively. It has been shown that as the work function of the gate increases to Φ_1= 4.6eV, the OFF state leakage current decreases.

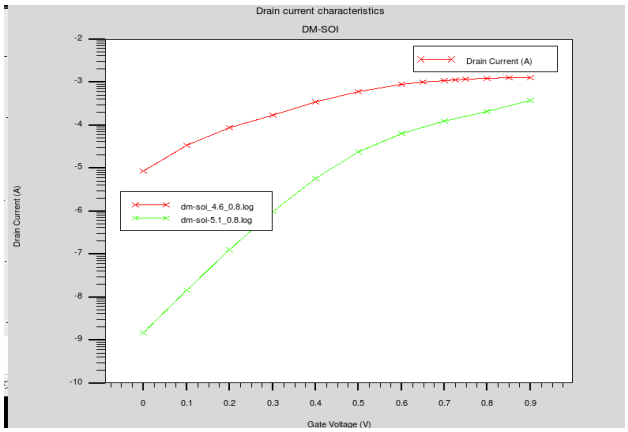

Fig. 5. I_{DS}-V_{GS} characteristics at different work-functions

The I_{DS}-V_{GS} (Drain-to-Source Current vs. Gate-to-Source Voltage) characteristics of a MOSFET can vary with different work functions, particularly in the context of the gate material. The work-function difference between the gate material and the semiconductor affects the threshold voltage and overall behavior of the transistor. Different gate materials with varying work functions can alter the shape and characteristics of the I_{DS}-V_{GS} curve. A higher work-function gate material tends to shift the entire curve in the positive V_{GS} direction, while a lower work-function gate material shifts it in the negative V_{GS} direction. This shift influences the operational range of the transistor for a given V_{DS}. While the thin-film thickness is decreased, the front-gate control over the surface of the channel is increased as compared to the impact exerted by the source/drain. For distinct silicon film thicknesses i.e. t_{si}=9 nm and t_{si}=10 nm, the OFF-state leakage current is also calculated. For t_{si}=10nm, the leakage current is found to be lowered and increases with the rise in the thickness of silicon as shown in Figure 6 below.

The I_{DS}-V_{GS} (Drain-to-Source Current vs. Gate-to-Source Voltage) characteristics of a MOSFET can be affected by changes in the silicon thickness, particularly within the channel region where the current flows. Changes in silicon thickness can affect the subthreshold slope, which characterizes the off-state behavior of the transistor. Thinner silicon layers generally exhibit steeper subthreshold slopes, influencing the transistor's efficiency in low-power applications. The performance characteristics of the Dual material Gate (DMG) and Single material Gate (SMG) SOI devices are compared for the channel length L=15nm. The work function of the gate material is selected as 4.1 eV for SMG SOI. The channel concentration of the Single material (SMG) SOI device is therefore taken as N_A=1x 10^{15} cm^{-3}, which produces the same threshold voltage, Vth =0.21 V, for both the Dual material DMG and Single material SMG MOSFETs. The comparison of Single and dual material gate devices is done based on leakage current. It has been found that DM-SOI has less leakage current compared to SM-SOI MOSFET as depicted in Figure 7.

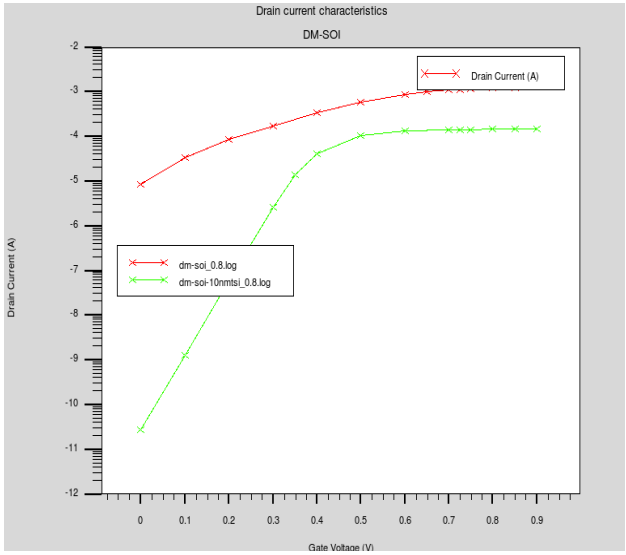

Fig. 6. I_{DS}-V_{GS} characteristics at different silicon thickness

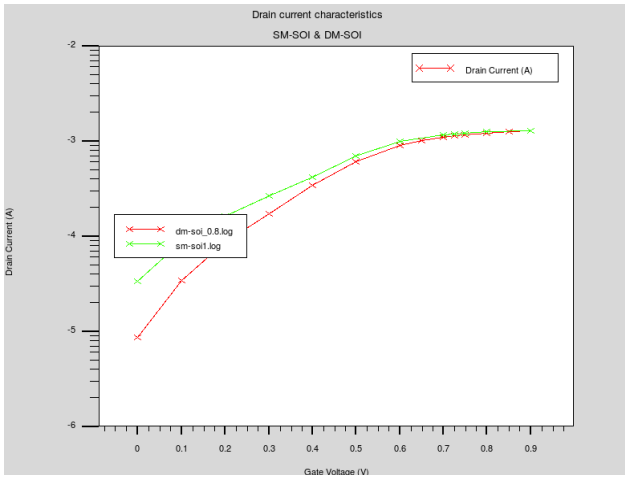

Fig. 7. Comparison graph of SM-SOI & DM-SOI MOSFET

SM-SOI MOSFETs have a single layer of silicon in the channel region. The reduced silicon thickness in SM-SOI MOSFETs can result in lower leakage currents, as shown in Figure 7. DM-SOI MOSFETs incorporate a thin layer of insulator with two silicon layers, creating a double channel. DM-SOI MOSFETs offer improved electrostatic control due to the presence of the buried oxide layer, which helps minimize short-channel effects and improves performance. By solving the 2-D Poisson equation under adequate boundary conditions, a two-dimensional analytical model of

surface potential for a Dual-Material Gate (DMG) SOI MOSFET can be obtained. The influence of various MOS parameters i.e. silicon film thickness, work function, applied drain voltages and effect of single & dual material gates on the leakage current, has been studied. In comparison with 2-D TCAD simulations, the results estimated by the model are validated. An additional point of choice for the design of the SOI transistor is the combination of Gate material engineering and Channel engineering, a good outcome discussed by this formulation [12,13].

4. Dual Halo Dual material SOI MOSFET

The dual-material SOI structure developed in the above section does not offer good results in terms of leakage current. The idea of halo doping comes into the frame, either single or double to enhance the performance of the device. The doping is performed on one side of the channel in single halo dual material SOI MOSFET (SHDM-SOI) MOSFET to improve the efficiency of the device. The halo doping is performed on both sides of the channel in the Dual Halo Dual Material SOI device so that the best leakage current value can be obtained for low-power applications. The Channel Engineering approach such as the Single-Halo (SH) also known as the lateral asymmetric channel or Dual-Halo (DH) implants is utilized to minimize the short channel effects [18]. To produce a novel device structure, such as the Dual Halo Dual Material Gate (DHDMG) MOSFETs, channel engineering and gate engineering methodologies are merged. By adding impurities from both the source and drain areas, pocket implantation causes the reverse short-channel effect (RSCE) [19,20]. As the pocket length increases, pocket doping gradually decreases linearly from the source and drain areas to the substrate concentration.

4.1 Device Fabrication

The Dual Material Dual Halo MOSFET (DMDH MOSFET) is an advanced type of Metal-Oxide-Semiconductor Field-Effect Transistor designed to enhance device performance by combining different materials and halo doping techniques in its structure. Here's a simplified and generalized fabrication process for a Dual Material Dual Halo MOSFET: The first step is Substrate Preparation having a silicon wafer substrate of high purity. The second step is Isolation which uses techniques like shallow trench isolation (STI) to isolate individual transistor regions. The third step is Gate Formation in which a thin layer of silicon dioxide (SiO2) as the gate oxide is deposited and a layer of polysilicon or metal to form the gate electrode is deposited patterned. The fourth step is Halo Doping in which an ion implantation technique is used to introduce dopants (boron for p-type, phosphorus for n-type) around the source and drain regions. Dual halo doping involves two separate doping steps with different energies and doses for the p-type and n-type regions. The fifth step is Source/Drain Formation used to define the source and drain regions by ion implantation, doping them differently for n-type and p-type regions.

The sixth step is Dual Material integration used to implement different materials for the source/drain regions, possibly using selective epitaxy or metal alloying techniques to enhance carrier mobility and to introduce high-k dielectrics as gate insulators to improve gate capacitance and device performance. The seventh step is Annealing and Activation used to subject the wafer to high-temperature annealing to activate dopants and repair crystal lattice damage caused by ion implantation. The eighth step is Dielectric and Metal Deposition, used to deposit additional dielectric layers for insulation and planarization, and pattern and deposit metal layers for interconnections and contacts between different parts of the MOSFET. The ninth step is Etching and Cleaning, which includes photolithography and etching techniques to define and shape the various layers and to clean the wafer thoroughly between steps to remove residues and contaminants. The tenth step is Testing and Packaging is to perform electrical testing on fabricated devices to assess functionality and performance and then Cut the wafer into individual chips and package the MOSFETs, ensuring they are protected and ready for use.

4.2 TCAD Simulation Results

Figure 8 shows the structure of the Dual Halo Dual material SOI MOSFET material with dual halo doping on both sides of the channel.

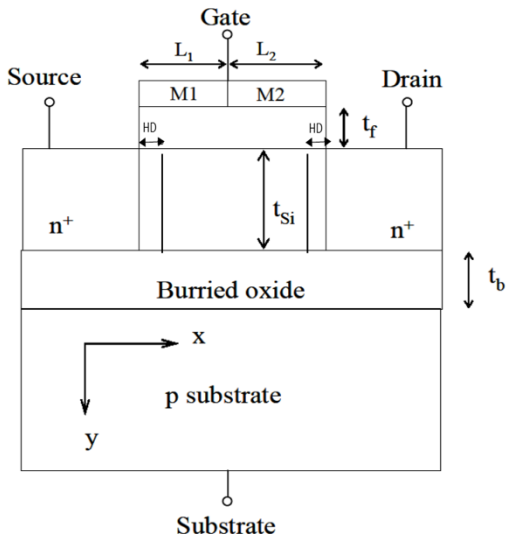

Fig. 8. DHDM-SOI MOSFET Structure

The simulations are carried out using TCAD software and the drain current characteristics are plotted. The device is designed with a single halo doping and a dual halo doping in the channel region and their characteristics have been compared. The optimized halo doping facilitated the device to be used in low-power applications [21]. The velocity of the electrons in the form of impurity scattering along the channel was reduced by the use of doping engineering in this optimized device resulting in less impact between electrons and atoms in the DHDM-SOI device [22,23].

Dual Halo DM-SOI typically demonstrates better electrostatic control and reduced short-channel effects due to the presence of dual halo structures and additional gates [24]. Both types can offer improved current modulation and reduced leakage compared to conventional MOSFETs, but Dual Halo DM-SOI may showcase even more enhanced characteristics due to its advanced structure [25]. The comparison of drain current with single halo doping and dual halo doping in the channel has been observed in Figure 9 in linear mode.

The choice between Single Halo DM-SOI and Dual Halo DM-SOI often depends on specific performance requirements, technological constraints, and manufacturing feasibility. Dual Halo DM-SOI, with its additional gates and dual halo structures, might offer superior performance but could also be more complex to fabricate compared to Single Halo DM-SOI. Dual Halo DM-SOI offers better mitigation of

short-channel effects compared to Single Halo DM-SOI due to the dual halo structures and additional gates [26]. The presence of two halo structures and two sets of gates allows for superior electrostatic control, reducing short-channel effects more effectively than Single Halo DM-SOI. The additional gates in Dual Halo DM-SOI offer increased control and modulation capability over the channel, potentially improving performance parameters [27]. DHDM-SOI has less ON current and less OFF-state current as shown in Figure 10 in logarithmic scale.

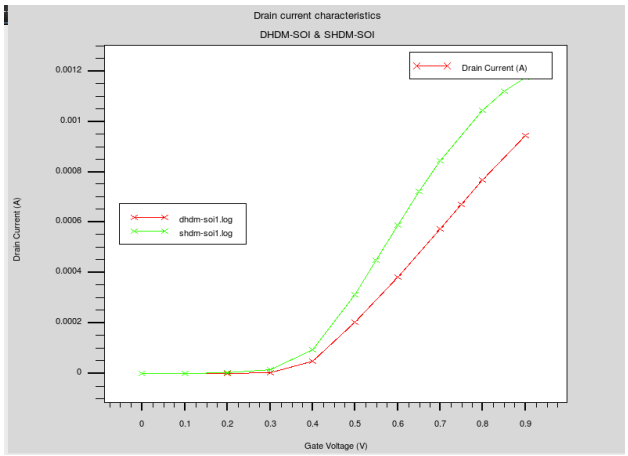

Fig. 9. Drain current characteristics of SHDM-SOI & DHDM-SOI

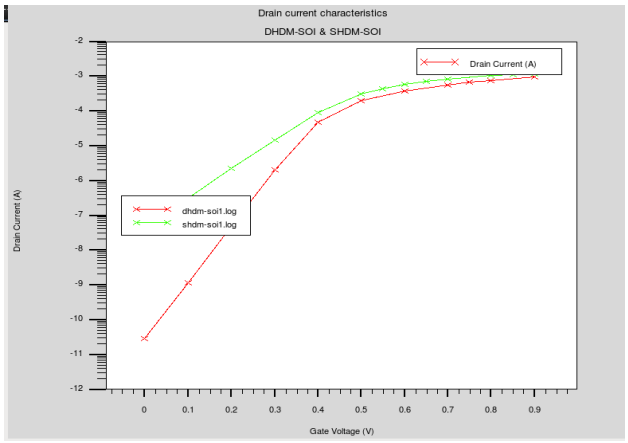

Fig. 10. Comparison graph of SHDM-SOI & DHDM-SOI MOSFET

Dual Material-SOI focuses on improving carrier mobility by using alternative materials in the channel, potentially resulting in higher drain currents and enhanced performance. Single Halo DM-SOI offers improved gate modulation and reduced short-channel effects due to the halo doping and dual gates, enhancing overall performance and control. Dual Halo DM-SOI provides superior short-channel effect suppression and enhanced gate control, especially beneficial for advanced technology nodes, owing to the presence of dual halo structures and additional gates [28]. Dual Halo DM-SOI, with its multiple gates and dual halo doping, offers superior performance at advanced nodes, while Dual Material-SOI improves carrier mobility and overall transistor performance. Figure 11 below shows the drain current characteristics of the dual material SOI (DM-SOI) MOSFET, single halo dual-material (SHDM

It has been observed that Dual material (DM–SOI) MOSFET is the best device in terms of drain current and Dual Halo Dual Material (DHDM–SOI) MOSFET is best in terms of sub-threshold leakage current as observed in Figure 12 in logarithmic scale.

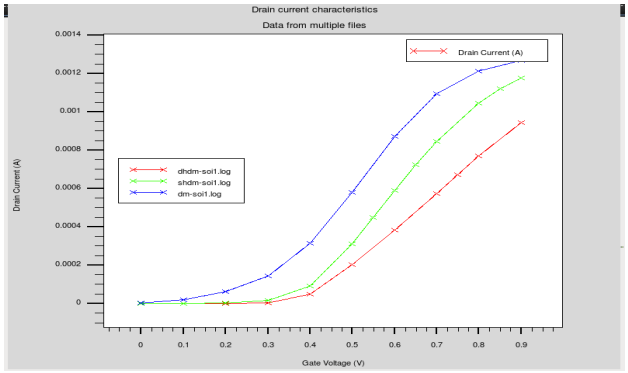

Fig. 11. Drain current characteristics of DM-SOI, SHDM-SOI & DHDM-SOI

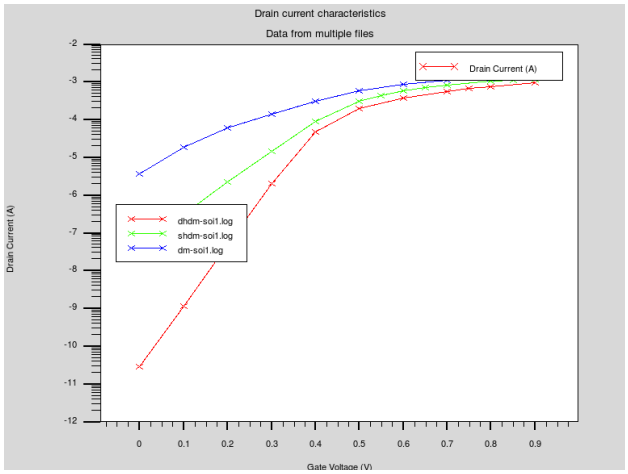

Fig. 12. Comparison graph of DM-SOI, DMSH-SOI & DMDH-SOI MOSFET

Table 2. Comparison of Simulated SOI Device Results with Literature

S.No.	Parameter	Karbalaei et al .[29]	Simulated Data
1.	Sub-threshold current	0.44 e-9 A	2.89 e-11 A
2.	Drain Current	0.23 mA	0.94 mA
3.	Ion/Ioff Ratio	53 e+4	32.6e+06
4.	SS (mV/dec)	74	61.5

Table 2 shows the comparison of simulated device data with the previous work done.

5. Conclusion

In this chapter, Dual material SOI (DM-SOI), Single Halo Dual material (SHDM -SOI) and Dual Halo Dual material (DHDM -SOI) have been investigated. Along the channel, the surface potential is estimated analytically and simulated at various drain voltages. For each of these devices, estimations have been obtained for the drain current, sub-threshold leakage current, ON/OFF ratio, and sub-threshold swing. The leakage current of 2.89x10-11A, ON/OFF ratio of 32.6e+06, and Subthreshold Swing of 61.5 mV/dec are observed to be the optimum values for DHDM-SOI MOSFETs. The proposed device, when compared to the literature, has a high ON/OFF ratio and low leakage current, making it ideal for low-power applications. DM-SOI MOSFET, however, provides the best value of drain current at 1.26 mA. Variations

in the silicon film thickness, work function, and drain bias all have an impact on the device's sub-threshold capabilities. When compared to two screen gates, it has been found that the device is more stable when the control gate's length is extended.

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