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Review Article

Single Event Upset Detection and Hardening schemes for CNTFET SRAM – A Review

T.R.Rajalakshmi[1] and R.Sudhakar[2]

[1.] *Department of Electronics and Communication Engineering, P.S.V College of Engineering and Technology, Krishnagiri, Tamilnadu, India.*
[2] *Department of Electronics and Communication Engineering, Dr.Mahalingam College of engineering and Technology, Udumalai road, Pollachi, Tamilnadu, INDIA.*

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Abstract

Carbon nanotubes (CNT) provide a better alternative of silicon, when it comes to nano scales. Thanks to its high stability and high performance of carbon nanotube, CNT based FET (CNTFET) devices which are gaining popularity of late. Single Event Upset (SEU) in a device is caused due to radiation. Radiation can be through two ways, one due to charge particles present in the atmosphere and other due to alpha particles. In this article we review some of the detection and hardening schemes in CMOS SRAM and make related simulations on CNTFET SRAM. The aim of this paper is to present the challenges the CNTFET SRAM is facing when the radiation effects are introduced. A full experimentation of all the schemes of detection and correction schemes will be beyond the scope, so only certain experiments that can be well carried out with CNTFET SRAM memory is more focussed.

Keywords: CNTFET SRAM, Built in current sensor (BICS) Radiation hardening, Single event upset.

1. **Introduction**

Carbon nano tube FET commonly called as CNTFET is a FET device which uses carbon nano tubes as channel instead of bulk silicon. CNTFETs possess the advantages of having good electrical properties, optical properties and they have good chemical stability. They exhibit ballistic transport over the lengths of several hundred nanometers. Soft errors are the major threat to devices. When we scale down the devices the impact of SEU is more .The SEUs are modelled as current pulses which has the varying amplitude based on the amount of charge.

Radiation induced errors causes the memories to function in a different way than expected. Now a days these types of errors bring serious issues, even in sea level. They were due to the ionizing particles in the space and also due to the alpha particles emitted from the unstable ions in packaging materials of the chips.

These particle strike result in the alteration of voltage values at the nodes [46].The impact of SEU in memories is that it can flip the values of the memory cell. In earlier methods which used Error control circuitry (ECC) had many disadvantages which include area overhead, power dissipation and performance. Further, the ECC's detected error not at the instant of SEU occurrence, but after the fault has occurred. Built in Current Sensors are used for the detection of SEUs at the instant of time they occur. SEUs can occur at any instant of time and hence asynchronous BICS is used for the detection. BICS is attached to the power lines of the memory device. Whenever radiation affects the cell abnormality in the current flow, it is detected through the Power lines and error signal is generated. This abnormality in the current flow, which is very small is amplified and is given to the latch through which the error signal is generated. There are various types of BICS circuits developed which includes the design of BICS to detect soft errors by [1]. This had some serious disadvantages with respect to voltage and temperature variations which were overcome in [2] and also the number of transistors was reduced. Later bulk BICS gained popularity due to its sensitivity in detecting a very small amount of current flow. And it added up with the advantage of occupying less area than that of the normal BICS [3] given in figure 4.Apart from the detection of soft errors several other BICS which is used to detect quiescent current have been studied in the literature. At the system level various error detection schemes are used to detect the flipping errors .The drawback of these is that BICS detected the errors at the time of occurrence, while Error detection schemes detect errors after the occurrence.

Soft errors can be overcome by several methods which includes hardening schemes and also by error correcting circuitries. The low cost scheme to protect the circuit from SEU's is to use error correcting and detecting codes. Hamming codes can be used for full protection [47].Radiation hardening refers to making the circuit tolerant to the radiation effects by introducing extra circuitry. Radiation hardening can be done through 3 ways, 1) through altering the physical components, adding bipolar or CMOS circuits and through error correction schemes [4].

Several error detection and correction circuitries had been developed. The aim of this paper is to compare the several techniques with respect to CMOS SRAM and extend the same for CNTFET SRAM. Along with the correction circuits fault tolerant design techniques are also used to reduce the impact of single event upset in SRAM.

* E-mail address: rajeereno@gmail.com
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The observations made for CNTFET SRAM is considered with write operation and for the SEU hitting the NMOS cell which brings about 1-> 0 transitions in Q.

The paper is organized as follows Section 2 reviews the single event upset concepts, section 3 reviews CNTFET, section4 deals with SEU Detection schemes, Section 5 deals with SEU hardening schemes, section 5 discusses the results and section 7 deals with the future research scopes.

2. Single Event Upsets (SEU)

2.1 Sources of Radiation

Two main sources of radiation are considered one is through the alpha particles from the naturally occurring radioactive elements.[5]. These elements when present during the packaging cause the faulty behavior.

Second source for radiation comes from the atmosphere, where cosmic ray induced neutrons cause the effect. The effect due to cosmic ray is more than that of the alpha particles.

And the third source which is least fixed is through the neutron induced fission. [6]

2.2 Effects due to SEU based on the Particles

Various types' defects are caused by different radioactive particles. The particles, which cause single event effects, include protons, electron heavy ions, cosmic rays and plasma electrons. Single Event latch up is the result of heavy cosmic rays. [7]. Single event upsets mostly result in transient faults.

2.3 Types of errors caused by Radiation

Based on the particle strike the errors can be classified into hard error and soft errors.

The types of error depend on whether it is permanent damage or temporary damage. Single event upsets come under the clause of temporary damage or soft errors. The affected circuits can be recovered by using reset signals or by correction circuits. Hard errors are due to permanent damages. These errors cannot be corrected or the circuits cannot be recovered by correction mechanisms Single Event Burnout (SEB), Single Event gate rupture (SEGR) and single event latch up (SEL) comes under this category [8].

In this review we are going to review about the Single Event Upset which is soft error and which occurs in memories. These SEUs cause transient errors in combinational circuits and makes bit flips in sequential circuits.

The CMOS SRAM basic cell is considered. An extensive study had been done with the detection and correction schemes for 6T SRAM cell. The similar simulations for CNTFET SRAM was done and compared with the same. Figure 1 shows the effect of single event upset in CNTFET SRAM.

Current testing is gaining more popularity in measuring the SEU defect since the SEU causes a small amount of leakage current to flow which alters the vdd and gnd supply. Some of the current based testing methods are by using IDDQ methods, dynamic testing methods and the measuring current through the bulk. The single event upsets have been modelled as a current pulse.

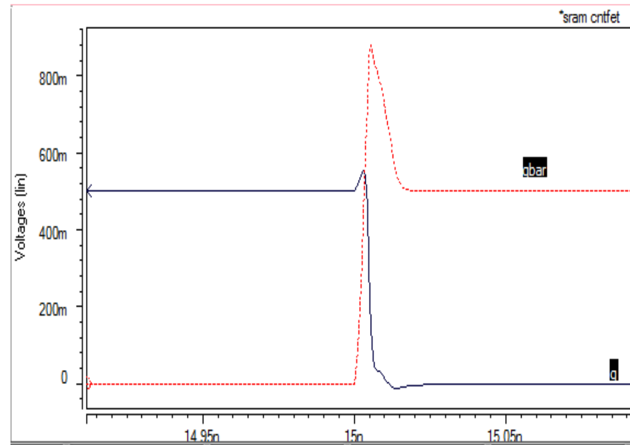


Fig. 1 shows the effect of single event upset in CNTFET SRAM.

3. CNTFET

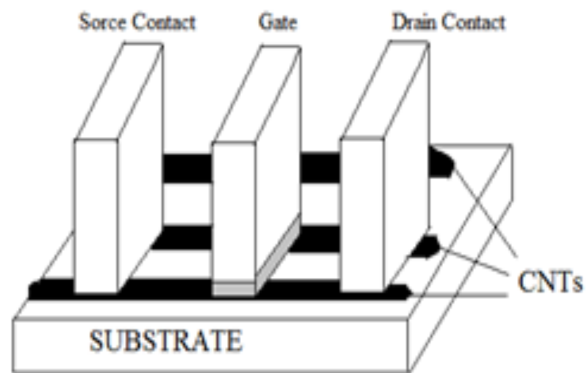


Fig. 2. The arrangement of CNTS in CNTFET.

Figure 2 shows the arrangement of CNTS in CNTFET.Carbon nanotube FET devices pose a challenging future by replacing CMOS devices. They possess promising characteristics which make them superior to CMOS devices. Various factors which influence the radiation effects in CNTFET have been studied. This includes CNTFET materials, chiral angles, temperature effects, and resistive defects.

Their electrical and mechanical properties seem to have more advantages than CMOS SRAM. They can be made to work as a nano wire or as a semiconductor by changing their chiral and diameter values.[9][10].

The effect of channel length variation is dealt in [11] which conclude that higher channel length results in good mobility characteristics. The variations in channel length also have a greater effect in the characteristics of CNTFET.The characteristic comparison between CMOS SRAM and CNTFET SRAM have been analysed in[12].It has been experimented that CNTFET shows less amount of leakage compared to normal SRAM.

Hence during the study of effect of SEU in CNTFET SRAM the parameters such as diameter, chiral values and channel length were varied the effects were studied. Figure 2 gives the dependency of charge values on the diameter of CNTFET.

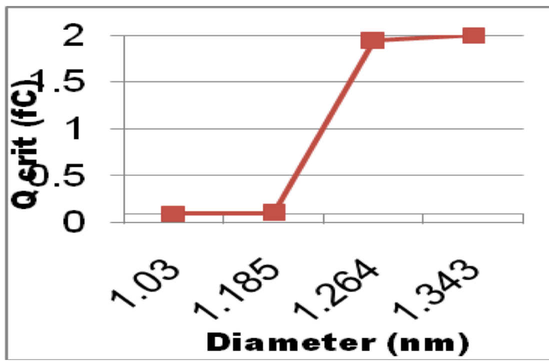


Fig. 3 shows how the charges are dependent on diameter values of CNTFET

The various defects in CNTFET results in the occurrence of faults. [13].The manufacturing defects which includes metallic defects open defects, poor contacts result in resistive shorts, channel resistance variation and threshold voltage variation. CNTFET has mostly stuck faults at the transistor level due to their similarity with MOSFETS. The opens and misalignment in CNTs result in the loss of memory behaviour which may lead to incorrect read and write faults. This analysis of defects in CNTFET SRAM helps to study the effect of SEU in CNTFET in the presence and absence of Resistive open and bridging defects.

Choice in the selection of CNTFET base materials is a promising fact, when compared to CMOS devices. The effect of cosmic radiation is much reduced in new nanometric devices due to use different kind of materials when compared to the standard CMOS circuits. [14]

The effect of variation in temperature on the performance of CNTFET is experimented in [15], which shows that, when the temperature is increased the current ratio with respect to on off conditions decreases. Also the temperature has greater impact on the drain conductance and sub threshold swing. This dependency of temperature has also been experimented for CNTFET in the presence of SEU and the results were observed. From the results, as the temperature rises, the effect of SEU in flipping the cells is reduced, compared to that in low temperatures.

The single event upset have been analysed in CNTFET SRAM and it showed less leakage of current compared to CMOS SRAM. The leakage current also showed dependency on diameter and chiral factors. Hence the development of a novel built in current sensor and special hardening schemes are necessary to detect and correct SEU in CNTFET SRAM.

4. SEU Detection Schemes

4.1 CMOS SRAM

SEU detection in this paper has been reviewed at circuit level.

Transient current testing method is employed for the detection rather than Quiescent current since it possesses the advantage of being used for dynamic study.

Built in Current Sensors are normally employed for the detection of Single event upsets. The basic idea behind the usage of BICS is the detection of flow of current in the SEU affected transistor which disturbs the power and ground supplies. The advantage of BICS over Error Detection Circuits (ECC) is the instantaneous detection of error rather than detecting it after the occurrence. ECC's causes area overhead and it reads the error after certain time. So there exists latency in the detection of errors. Built in current sensors are used for fault detection in memory circuits and also for SEU detection.

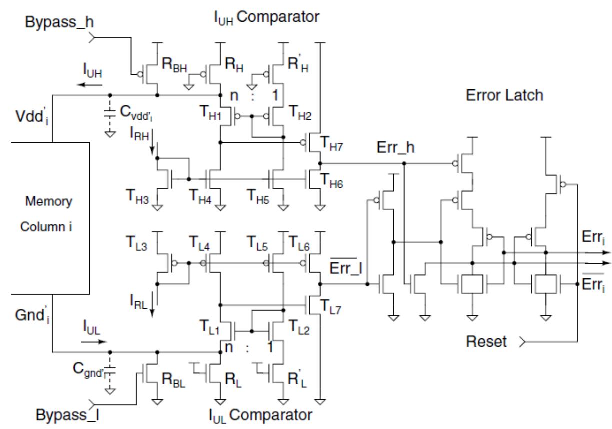


Fig. 4. BICS proposed by [3]

In this section we review the BICS used mainly for SEU detection

Normal BICS were designed to detect the current fluctuations at static condition these BICS had been given in [2].

Bics proposed in [2] was designed to detect SEU and it was based on the current monitoring.

The BICS proposed by [1] given in figure 5 has the advantages of voltage monitoring rather than current monitoring, with less number of transistors. And also it is validated for different shapes of current pulses. This design used two current comparators and an asynchronous latch. For 1->0 flipping the SVDD part detects the flipping while 0->1 transition is detected by Sgnd .These supplies and grounds are formed using transistors MV1-MV8 and Sgnd is the counterpart of SVdd.

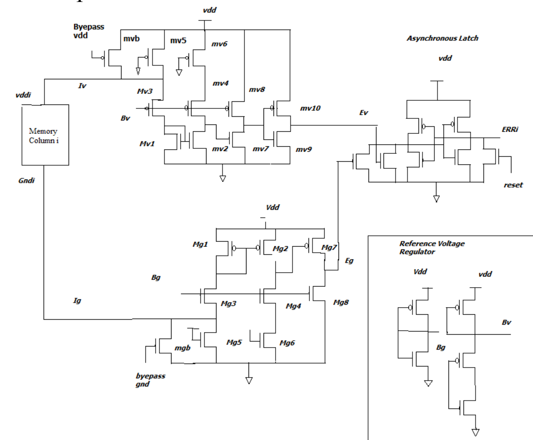


Fig. 5. Bics proposed in [1]

Improved version of [1], the BICS detection is proposed in both operating and in standby condition is experimented in [17]. In that the reset signal is controlled by a logic circuitry which makes it to work for all operating conditions.

BICS shown in figure 6 which is used to detect resistive defects can also detect SEU occurrence. The BICS is connected with cell arrays. The idea behind that is to combine algorithm such as the March along with BICS to give an effective solution. The combination reduces the number of March elements. With the introduction of BICS, WRITE operations are not affected while the read operations are affected. [18]

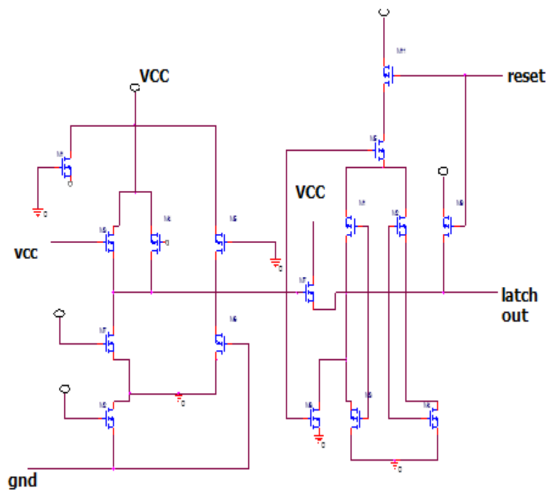


Fig. 6.BICS [18]

Built in current sensors for the IDDQ detection is stated in [19]. Different types of methodologies were used which includes varicap thresholds approach and switched capacitor approach. The first one uses a fast comparator and two capacitive arrays. This uses domino logic, which includes precharge and evaluation phase.

In both, the advantage is being low area occupancy and less design complexity.

The differential amplifier concept poses an advantage of Column level error detection [20] and uses a differential amplifier and a current mirror for the detection of SEU. It had the advantage of detecting all spikes with less overhead. The developed bics was tolerant to PVT variations. In this method the detector was connected only to ground rail and not to power rails as in the previous methods. Column level error detection was done for memory arrays.

The next set of BICS schemes is based on bulk current detection.[21] Introduced the concept of bulk bics. In this bulk BICS detects the transition when the particle striking node reaches Vdd/2 or more. Bulk BICS [21] quickly responds to SEU when compared to previous works. It uses very simple bulk circuits. Bics for SRAM includes P-BICS and N-BICS separately for 0 to 1 and 1 to 0 detection. [22] describes the current sensor connected to the bulk terminal of NMOS and PMOS. This type of detection of SEU helps to differentiate between internal logic signals and SEU current signals. The value of bulk current flowing under normal conditions is very low and during the particle strike it is much higher. The BICS developed is evaluated at the device level.

Novel built in current sensor [23] advantages are operated in a wide range of temperature, process variations with less power dissipation when compared to other BBICS. It uses the concept of head and tail connections. Head generates the error signal and tail is designed in a way that works as asynchronous latch. [23]. When the particle strike happens, the output of head block becomes low and output is given to the input of an inverter and the latch, which enables the error signal to be high.[24] The built in current sensor for IDDQ measurement mainly focus on flip-flop operation. The sensing operation includes scan in, scan out and measurement modes. It provides the advantage of performance, accuracy and effectiveness.

Experiments in [25] deal with building new bics which is divided into N.-BICS and P-BICS. The sensor block consists of sensing cells and asynchronous latch. This also comes under the variety of bulk built in current sensor. It consists of eight transistors and is mainly designed for the detection of SEU in multipliers. Area overhead is reduced mainly in this design. [26] The bics scheme includes a calibration circuit along with the conventional current sensor. The purpose of the calibrated current to voltage converter circuit is to give the voltage output which represents the current value of circuit under test. Process variations which cause the deviations are managed well through the calibration circuit.

Next part discusses about the MAGFET based current sensors and its advantages.[27] The current sensor which is based on magnetic field senses the magnetic field and gives the corresponding electrical signal as output. It use the idea of transistor structure with split drains. Difference in output is observed with difference in MAGFET cells. These type sensors provide higher sensitivity.

In this section, certain bics sensors experimented with CNTFET SRAM and it shows the relative comparison.

4.2 CNTFET SRAM

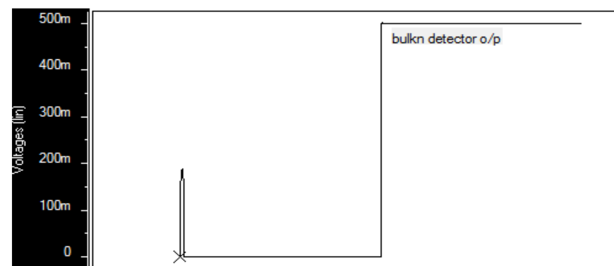
4.3 Comparison of results

The comparator based detection scheme developed by [20] gave the error detection signals for higher leakage currents. When CNTFET is considered the flip in output causes very less amount current variation in ground rail which is not able to be detected by this scheme.

This design has been implemented with CNTFET SRAM. This design unlike the previous design is able to detect but only for higher leakage current. But the minimum leakage in vdd range is better compared to the previous design{29].[25] Is working best when compared to other detection schemes. This technique is able to detect for the bulk leakage current starting from 7uA. Also this technique possesses the advantage of inbuilt latch. But when using CNTFET with SEU the bulk leakage current comes around 250nA-500nA which is a very low current. Figure 7 shows the bics detection when the current pulse is 8uA.

Since bulk techniques seem to be more promising compared to the normal methods in current sensing, building up of new built in current sensor based on bulk techniques has been studied for CNTFET SRAM.

The variation in m and n values CNTFET brings out variation in detection.



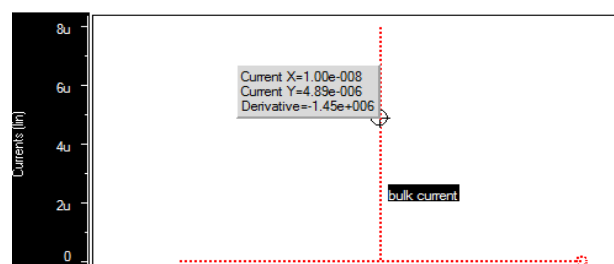


Fig. 7. Detection of leakage current up to 8uA

5. SEU Hardening Schemes

Hardening schemes refer to making the system more protective by adding external circuits or using codes such that the impact of SEU will not be observed in the output of a circuit.

The error is automatically corrected by the correction schemes.

SEU hardening schemes are done at different levels, physical, circuit and at logical level. Physical level hardening includes the correction methods by adding certain elements in the substrate. Error correction codes are done at system level, which includes many type of coding techniques. They are single error correction codes, double error correction codes, RS codes, BCH codes.

5.1 CMOS SRAM

The radiation hardening scheme is classified into two different categories. Physical radiation hardening and logical radiation hardening techniques. Physical radiation hardening scheme includes insulating substrates, use of bipolar elements as the principal elements since they are less affected by SEU compared to CMOS, use of wide band gap substrate, shielding the chips with depleted boron and the use of high Z materials. [4].

Logical hardening methods include the use of error correcting codes, using watchdog timers and by using redundancy elements.

In [47] new method of hamming code checks the multiple column data with improved speed. [30] Elaborates the usage of magnetic flip-flops. The advantage of magnetic memories is being very much resistant to radiation. The hiding concept is the magnetic tunneling junction which is referred as MTJ. In this write line is not physically shared by more than one fliflop. The MTJ elements provide isolation between storage nodes and the resistance to SEU is increased [31]. The technique is based on the linear code. This code detects and corrects single event upsets in random logic. It shows the advantage of having less hardware. It uses the concept of recomputation which is the key factor in the reduction of hardware. For error detecting and correcting codes, it uses modulo-2 arithmetic for checksum of n-bit register and for the error correction bit flipping latches is used.

An efficient hardening scheme based on current monitoring was proposed in [29]. This scheme has the combination of current monitoring and parity checking. BICS detects the abnormal current flow due to Single Event upset in RAM columns and parity check is used to correct the errors. It possesses sensing cell with an asynchronous latch for dynamic operation. This model has the advantage of less hardware and zero latency time. The disadvantage being noted is not applicable for combinational circuits.

A gate level radiation hardening scheme is given by [32] is based on dual modular redundancy so that the advantage is less area and less power consumption. This uses a special clock gating, which differs from normal gating schemes with the use of one more latch and an extra input to the gate. The proposed method is able to recover from 99% of SEU errors. Single Event effect in analog to digital converters is detected and corrected by multipath ADC technique. It possesses the advantage of real time correction, reusability and digital detection. [33].It concludes that digital detection is more efficient in detecting SEU's rather than analysing voltage and current waveforms.

Dynamic logic circuits [34] used for SEU hardening takes three different forms. The first type works in precharge as well as in the evaluation phase. The disadvantage of the circuit is, if two SETs occur sequentially either in precharge phase or in evaluation phase it produces erroneous output. The drawback is overcome by another circuit which includes two PMOS and two inverter circuits before the output terminal. This gives protection against multiple node upset. The increased power consumption is the disadvantage being noted. The third circuit shows the advantage of having reduced area by reducing the number of transistors and inverters. These dynamic circuits' have more advantages over TMR (Triple Modular Redundancy) schemes.

Error detection and correction methods for multiple bit upset includes single bit error correction and double bit error correction.. [35].Codes is represented in the form of Matrix. These codes are detected up to eight errors in a row with the condition that there should not be any error in the column. The results showed improved performance over hamming codes. [36] Introduces parallel implementation for Double Error correcting codes to overcome the traditional BCH and hamming code disadvantages. Reduced latency is observed in these codes when subjected to SEU. The parallel implementation is done with DEC-BCH codes.

A new hardening scheme based on dual modular redundancy uses Muller c-element to prevent the effects caused by single event upset. [37] By using internal feedback lines this scheme avoids the use of vulnerable internal nodes. The proposed scheme has the advantage of area efficiency and power efficiency over triple modular redundancy scheme. [38]Three traditional methods of hardening scheme were proposed; new approach with some modifications mainly deals with latches rather than with memories. It uses transistors of same size with gate array concept. This brings out changes in transistor connections and thereby improving the quality of the operation. These designs provide least power dissipation compared the traditional designs. In [39] the concept of partial decoupling architecture is used to increase the efficiency. Additional storage cell has been added to improve the decoupling. Double DICE owns the advantage of reduced charge sharing and collection in traditional DICE. Here sensitive nodes are separated by the introduction of new DICE. [40]

Another method of hardening includes critical charge value reduction [41] the critical charge value was reduced by combining the transistors of different threshold voltage values. In the earlier methods, width and length were adjusted which had the disadvantage of misalignments. [42] In this method the disadvantage of introduction of capacitors have been eliminated by introducing two CMOS transistor and a single capacitor. Capacitor acts as a charge buffer in the case of being affected by SEU.

The next hardening method [43] gives the development of new SRAM cell with 10 transistors and stacked mode for SEU hardening. In this method same potential nodes are kept apart, the disadvantage being the reduction in hardening when the voltage is reduced to sub threshold voltage. While the previous works on this focus on PMOS stacking this work focuses on NMOS stacking.

The addition of Miller capacitor in the feedback improves the radiation hardening. This uses the RADTRAPB design with improved PMOS features. In architectural level, the chip is divided into blocks and arrays. The array concept is used for storing the bits. Since, the chip is divided into blocks the case is reduced to single bit being affected. And the affected byte is recovered using

ECC [44].The schematic level hardening is achieved by decreasing the number of floating gates, restricting the pass transistor and increasing the parasitic capacitance. At layout level edgeless transistors are used to avoid thick oxides. The high-k dielectrics although preferred to control gate leakage and to have low oxide thickness, when they come for radiation effects it will be failed. High-k dielectric devices show higher degradation with radiation effects when compared to normal devices. [45]

The concept of DICE is proposed in [48].The number of transistors is the main disadvantage. In most of the cases, the number of transistor is used twice for achieving the radiation. In this, hardness is achieved by the additional transistors which drive the output to the previous state. The superiority of HIT cell which compared to other methods is given by [49].

The hardening scheme [28] used thirteen transistors. When compared to DICE it keeps the advantage of less performance degradation. This scheme is close to that of [52] which helps gate control voltages vp and vn. They help to restore the values of affected nodes by blocking them and getting the values from unaffected nodes. Signal generation and distribution are the disadvantages being noted. This has been corrected in [28] with different configuration. The cause of soft errors due to transient errors in the nodes [51] is corrected by the design of two hardening schemes. The first approach of hardened latch filters out the transition faults from entering into internal nodes. Previous designs focused on adding capacitance [53] and for filter, adding RC filters [54] resulting in more area and power consumption. Duplicating the nodes within the latch is considered as first hardening approach for filter the TFs which cause Soft Errors. The second approach has the advantage of high robustness by turning off the transistors when switching is done for 0->1.

5.2 CNTFET SRAM

Some of the hardening schemes have been experimented with CNTFET SRAM.

The introduction of MILLER capacitance is applied in CNTFET SRAM, the results showed that they prevented the flipping but haven't completely corrected the short pulse rise and settlement in output signals.

NMOS stacking concept experimented in [43][16] when applied in 6T CNTFET SRAM, the flipping of values is restricted for certain time period and after the values were retained. This scheme of hardening is comparably same as that of introduction of miller capacitance. Full stack method also results in the same hardening output as PMOS.

PMOS stacking haven't brought any hardening for Q 1-> 0 transitions.

6. Future Research

The review of various detection and hardening schemes makes it easy to design a novel BICS for the detection of single and multi-bit upsets in CNTFET SRAM. Various disadvantages which were observed in the previous designs paves way for a new design approach for CNTFET SRAM. Future research also includes the design of efficient error correcting schemes and circuit level hardening schemes for CNTFET SRAM. This study is planned to be expanded for multibit upsets also.

7. Conclusion

Single event upsets are a major concern in nano circuits. It affects the reliability of the circuit. Hence, it becomes necessary to detect and correct the errors. And in this nano era, as we move towards nanotubes, the study of these effects in CNTFET memories, detection and correction plays an important role. Since SRAM memories are used in space applications and also the main storage element, these effects in SRAM memories need attention. This paper gives a review about the BICS circuits and the radiation hardening schemes in SRAM. Some of these circuit level techniques are implemented by CNTFET SRAM and the results have been compared. Thus we understood that, CNTFET memories require special type of BICS and radiation hardening schemes compared to that of nano CMOS SRAMs.

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